

Bipolar Hall Latch

Hall Effect Latch for Industrial Applications

Product description

Overview



Characteristic	Supply Voltage	Supply Current	Sensitivity	Interface	Temperature
Bipolar Hall Effect Latch	3.0 V ~ 32 V	1.6 mA	B_{OP} : 2 mT B_{RP} : -2 mT	Open Drain Output	-40°C to 125°C



Figure 1 TLI4961-1M in the PG-SOT23-3-15 (left hand) and TLI4961-1L in the PG-SSO-3-2 (right hand) package

Features

- 3.0 V to 32 V operating supply voltage
- Operation from unregulated power supply
- Reverse polarity protection (-18 V)
- Overvoltage capability up to 42 V without external resistor
- Output overcurrent and overtemperature protection
- Active error compensation
- High stability of magnetic thresholds
- Low jitter (typ. 0.35 μ s)
- High ESD performance
- Leadless, non halogen-free package PG-SSO-3-2 (TLI4961-1L)
- Small, halogen-free SMD package PG-SOT23-3-15 (TLI4961-1M)
- For industrial and consumer applications, not qualified for automotive applications
For automotive applications please refer to the Infineon TLE Hall Switches/Latches series

Table 1 Ordering information

Product name	Product type	Ordering code	Package
TLI4961-1L	Bipolar Hall Latch	SP001052198	PG-SSO-3-2
TLI4961-1M	Bipolar Hall Latch	SP001031008	PG-SOT23-3-15

Product description

Target applications

Target applications for the TLI496x Hall Latch family are all applications which require a high precision Hall Latch with an operating temperature range from -40°C to 125°C. Its superior supply voltage range from 3.0 V to 32 V with overvoltage capability up to 42 V without external resistor makes it ideally suited for industrial applications.

The magnetic behavior as a latch and switching thresholds of typical ± 2 mT make the device especially suited for the use with a pole wheel for index counting applications and for rotor position detection as in brushless DC motor commutation.

Table of contents

	Product description	1
	Overview	1
	Features	1
	Target applications	2
	Table of contents	3
1	Functional description	4
1.1	General	4
1.2	Pin configuration (top view)	4
1.3	Pin description	4
1.4	Block diagram	5
1.5	Functional block description	6
1.6	Default start-up behavior	7
2	Specification	8
2.1	Application circuit	8
2.2	Absolute maximum ratings	9
2.3	Operating range	10
2.4	Electrical and magnetic characteristics	11
3	Package information	13
3.1	Package outline PG-SOT23-3-15	13
3.2	Packing information PG-SOT23-3-15	13
3.3	Package outline PG-SSO-3-2	14
3.4	Footprint PG-SOT23-3-15	15
3.5	PG-SOT23-3-15 distance between chip and package	15
3.6	PG-SSO-3-2 distance between chip and package	15
3.7	Package marking	16
	Revision history	17
	Disclaimer	18

1 Functional description

1 Functional description

1.1 General

The TLI4961-1L/1M is an integrated Hall effect designed specifically for highly accurate applications with superior supply voltage capability and temperature stability of the magnetic thresholds.

1.2 Pin configuration (top view)

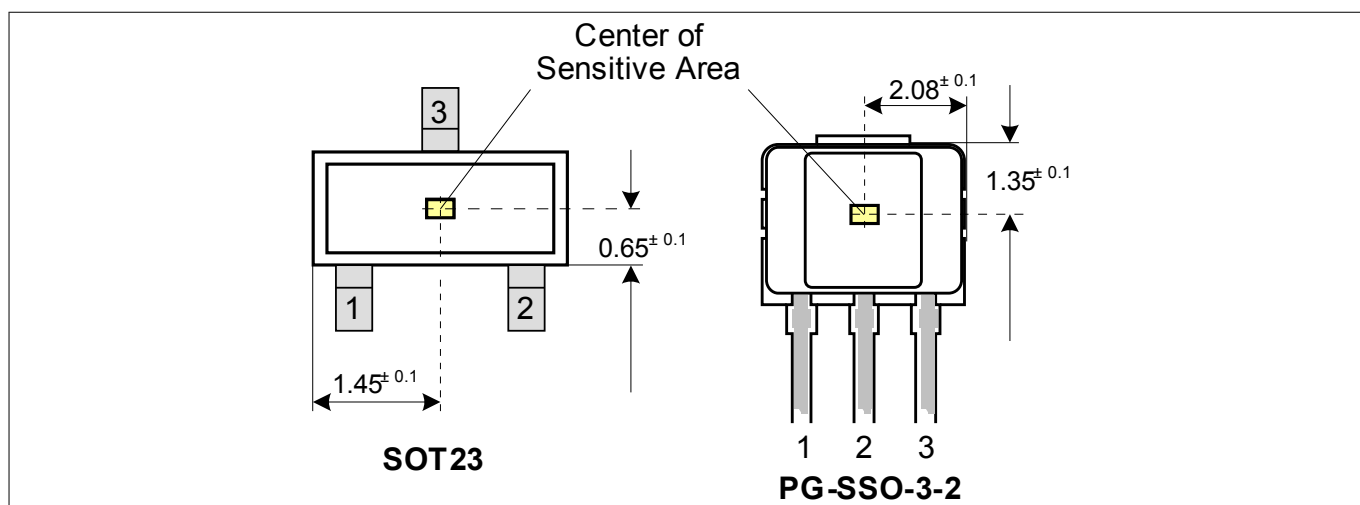


Figure 2 Pin configuration and center of sensitive area

1.3 Pin description

Table 2 Pin description PG-SOT23-3-15

Pin no.	Symbol	Function
1	VDD	Supply voltage
2	Q	Output
3	GND	Ground

Table 3 Pin description PG-SSO-3-2

Pin No.	Symbol	Function
1	VDD	Supply voltage
2	GND	Ground
3	Q	Output

1 Functional description

1.4 Block diagram

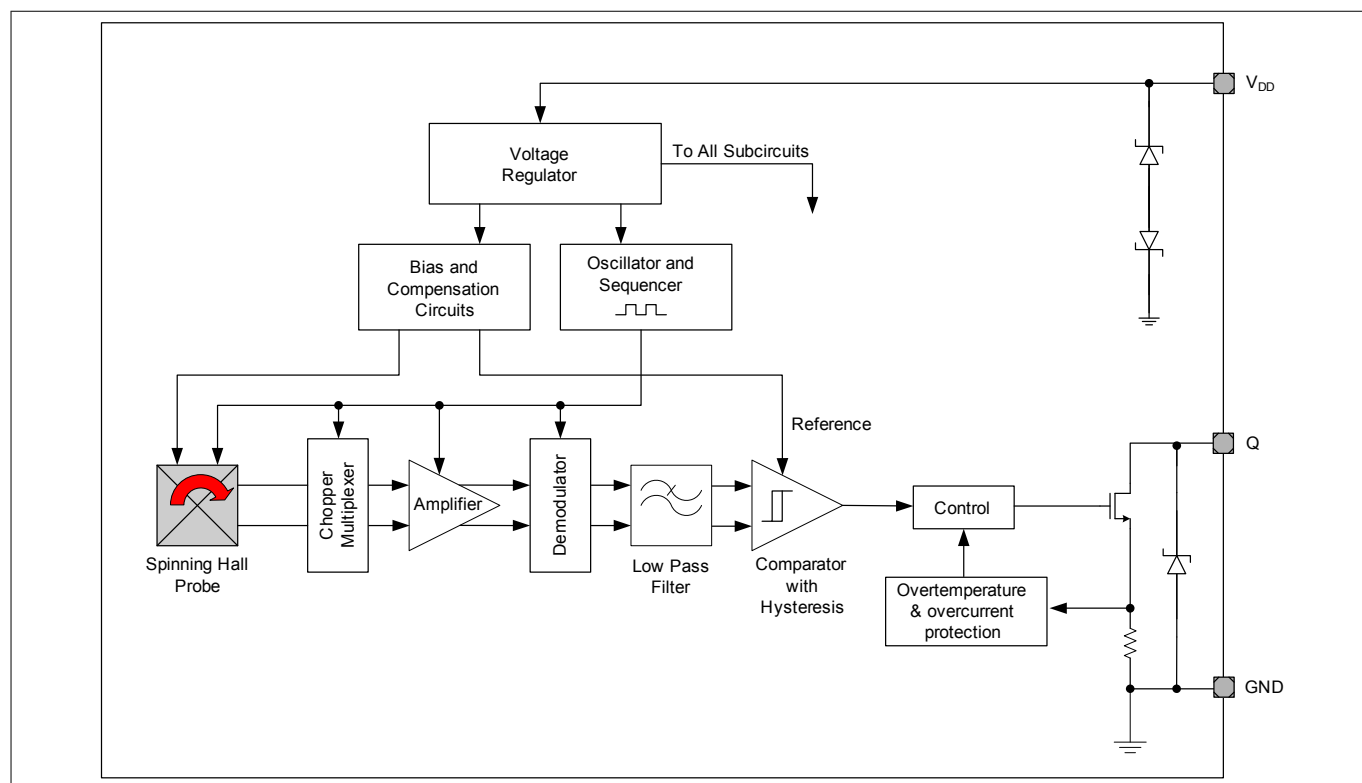


Figure 3 Functional block diagram TL14961-1L/1M

1 Functional description

1.5 Functional block description

The chopped Hall IC switch comprises a Hall probe, bias generator, compensation circuits, oscillator and output transistor.

The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce influence of technology variations.

The active error compensation (chopping technique) rejects offsets in the signal path and the influence of mechanical stress to the Hall probe caused by molding and soldering processes and other thermal stress in the package. The chopped measurement principle together with the threshold generator and the comparator ensures highly accurate and temperature stable magnetic thresholds.

The output transistor has an integrated overcurrent and overtemperature protection.

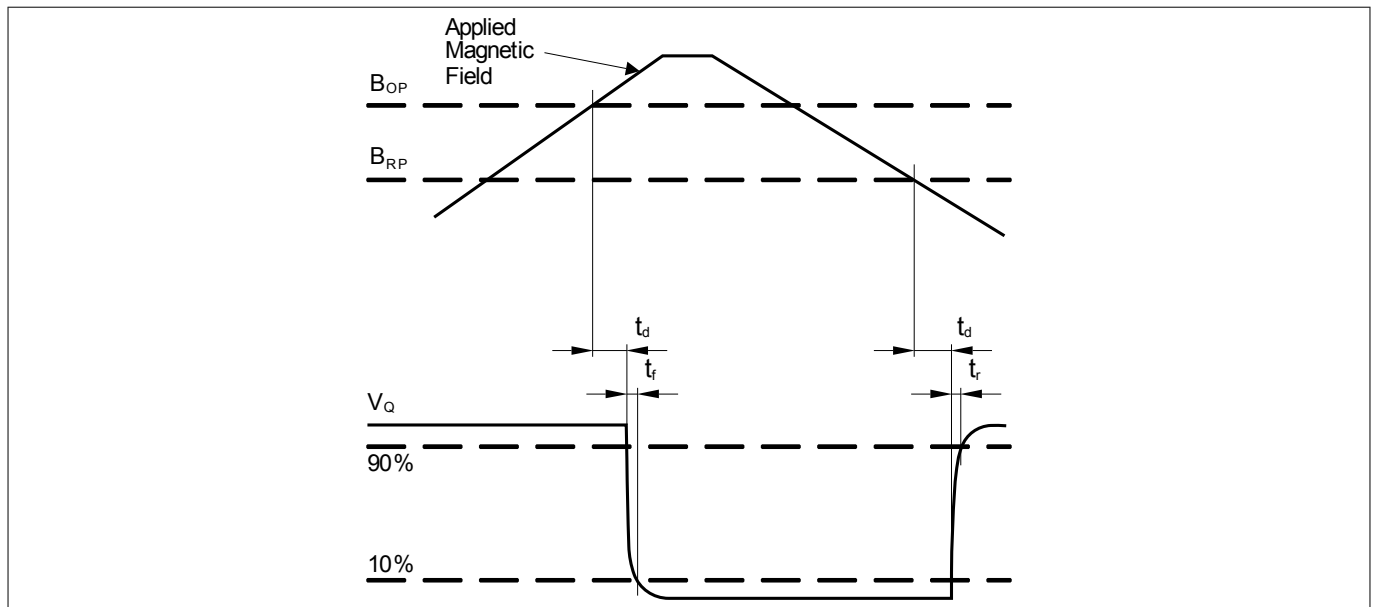


Figure 4 Timing diagram TLI4961-1L/1M

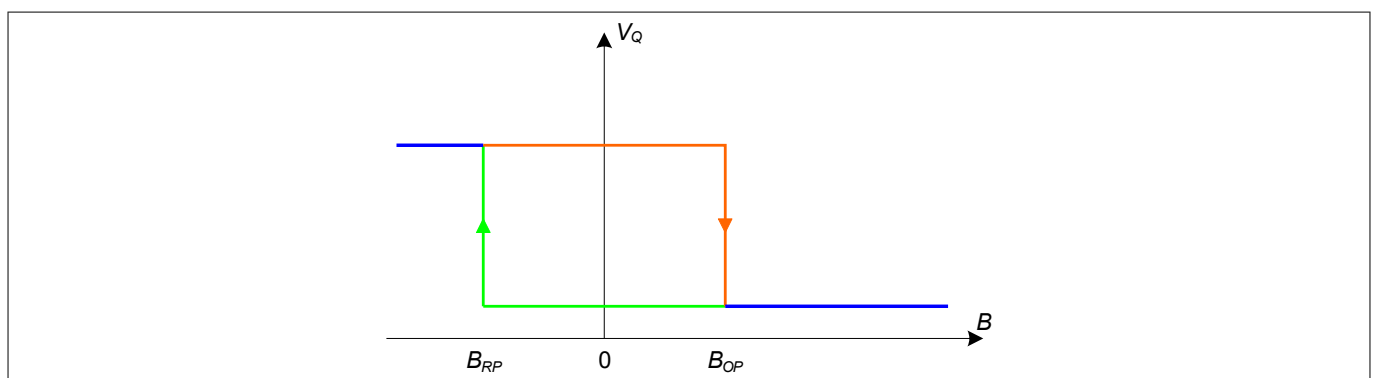


Figure 5 Output signal TLI4961-1L/1M

1 Functional description

1.6 Default start-up behavior

The magnetic thresholds exhibit a hysteresis $B_{HYS} = B_{OP} - B_{RP}$. In case of a power-on with a magnetic field B within hysteresis ($B_{OP} > B > B_{RP}$) the output of the sensor is set to the pull up voltage level (V_Q) per default. After the first crossing of B_{OP} or B_{RP} of the magnetic field the internal decision logic is set to the corresponding magnetic input value.

V_{DDA} is the internal supply voltage which is following the external supply voltage V_{DD} .

This means for $B > B_{OP}$ the output is switching, for $B < B_{RP}$ and $B_{OP} > B > B_{RP}$ the output stays at V_Q .

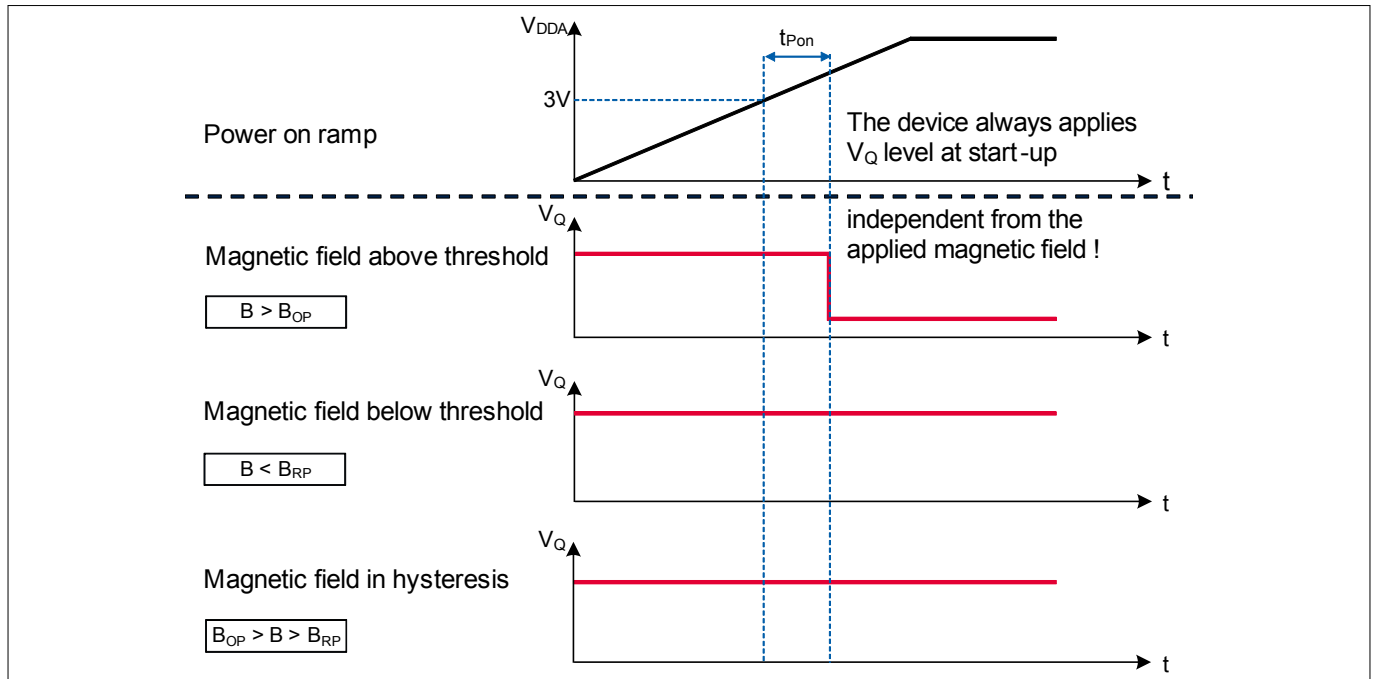


Figure 6 Start-up behavior of the TLI4961-1L/1M

2 Specification

2 Specification

2.1 Application circuit

The following [Figure 7](#) shows one option of an application circuit. As explained above the resistor R_S can be left out (see [Figure 8](#)). The resistor R_Q has to be in a dimension to match the applied V_S to keep I_Q limited to the operating range of maximum 25 mA.

e.g.: $V_S = 12\text{ V}$; $I_Q = 12\text{ V}/1200\ \Omega = 10\text{ mA}$

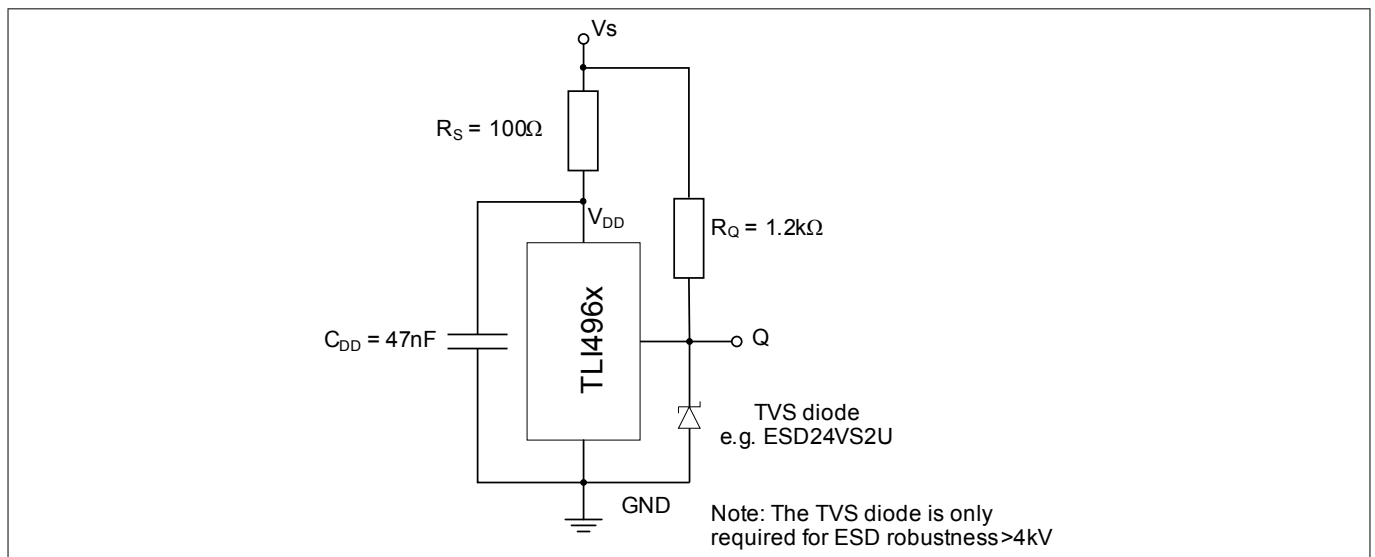


Figure 7 Application circuit 1: with external resistor

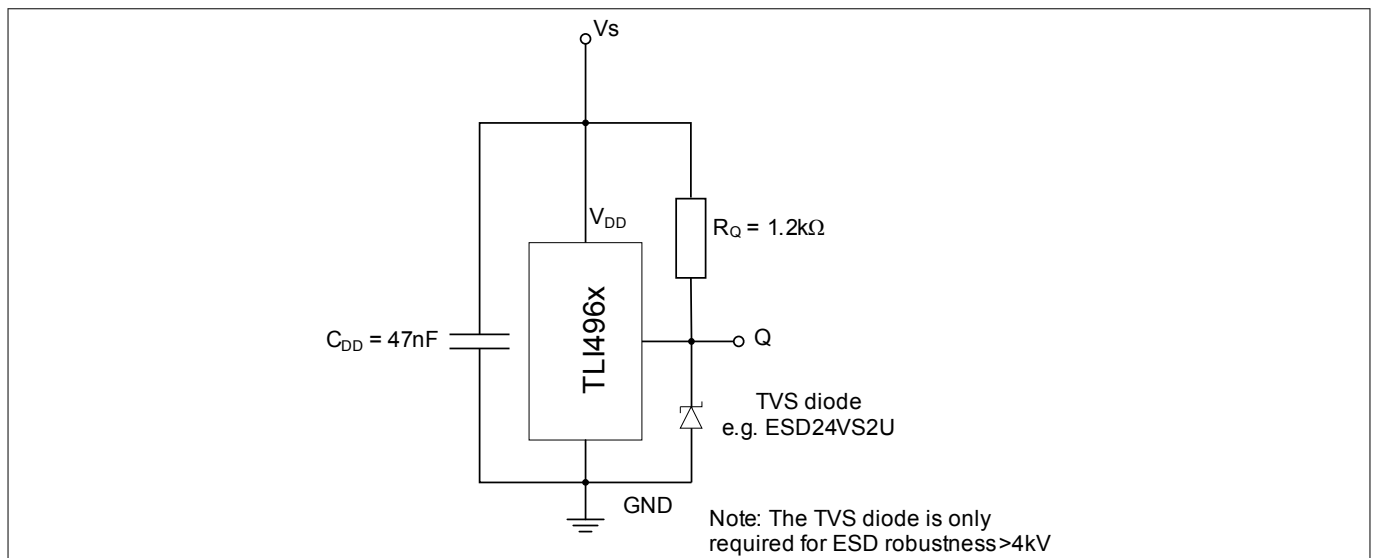


Figure 8 Application circuit 2: without external resistor

2 Specification

2.2 Absolute maximum ratings

Table 4 Absolute maximum rating parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage ¹⁾	V_{DD}	-18	–	32 42	V	– 10h, no external resistor required
Output voltage	V_Q	-0.5	–	32	V	–
Reverse output current	I_Q	-70	–	–	mA	–
Junction temperature ¹⁾	T_J	-40	–	150	°C	for 2000h
Storage temperature	T_S	-40	–	150	°C	–
Thermal resistance Junction ambient	R_{thJA}	–	–	300 200	K/W	for PG-SOT23-3-15 (2s2p) for PG-SSO-3-2 (2s2p)
Thermal resistance Junction lead	R_{thJL}	–	–	100 150	K/W	for PG-SOT23-3-15 for PG-SSO-3-2

1) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

Attention: *Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.*

Calculation of the dissipated power P_{DIS} and junction temperature T_J of the chip (SOT23 example):

e.g. for: $V_{DD} = 12\text{ V}$, $I_S = 2.5\text{ mA}$, $V_{QSAT} = 0.5\text{ V}$, $I_Q = 20\text{ mA}$

Power dissipation: $P_{DIS} = 12\text{ V} \times 2.5\text{ mA} + 0.5\text{ V} \times 20\text{ mA} = 30\text{ mW} + 10\text{ mW} = 40\text{ mW}$

Temperature $\Delta T = R_{thJA} \times P_{DIS} = 300\text{ K/W} \times 40\text{ mW} = 12\text{ K}$

For $T_A = 50^\circ\text{C}$: $T_J = T_A + \Delta T = 50^\circ\text{C} + 12\text{ K} = 62^\circ\text{C}$

2 Specification

Table 5 ESD protection¹⁾ ($T_A = 25^\circ\text{C}$)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
ESD voltage (HBM) ²⁾	V_{ESD}	-4	–	4	kV	$R = 1.5 \text{ k}\Omega$, $C = 100 \text{ pF}$
ESD voltage (CDM) ³⁾	V_{ESD}	-1	–	1	kV	–
ESD voltage (system level) ⁴⁾	V_{ESD}	-15	–	15	kV	with circuit shown in Figure 7 and Figure 8

- 1) Characterization of ESD is carried out on a sample basis, not subject to production test.
- 2) Human Body Model (HBM) tests according to ANSI/ESDA/JEDEC JS-001.
- 3) Charge device model (CDM) tests according to JESD22-C101.
- 4) Gun test (2 k Ω / 330 pF or 330 Ω / 150 pF) according to ISO 10605-2008.

2.3 Operating range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLI4961-1L/1M.

All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned.

The maximum tested magnetic field is 600 mT.

Table 6 Operating conditions parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	3.0	–	32 ¹⁾	V	–
Output voltage	V_{Q}	-0.3	–	32	V	–
Junction temperature	T_{J}	-40	–	125	$^\circ\text{C}$	–
Output current	I_{Q}	0	–	25	mA	–
Magnetic signal input frequency ²⁾	f_{SW}	0	–	10	kHz	–

- 1) Latch-up test with factor 1.5 is not covered. Please see max ratings also.
- 2) For operation at the maximum switching frequency the magnetic input signal must be 1.4 times higher than for static fields. This is due to the -3 dB corner frequency of the internal low-pass filter in the signal path.

2 Specification

2.4 Electrical and magnetic characteristics

Product characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production and correspond to $V_{DD} = 12\text{ V}$ and $T_A = 25^\circ\text{C}$. The below listed specification is valid in combination with the application circuit shown in [Figure 7](#) and [Figure 8](#).

Table 7 General electrical characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply current	I_S	1.1	1.6	2.5	mA	–
Reverse current	I_{SR}	–	0.05	1	mA	for $V_{DD} = -18\text{ V}$
Output saturation voltage	V_{QSAT}	–	0.2	0.5	V	$I_Q = 20\text{ mA}$
		–	0.24	0.6	V	$I_Q = 25\text{ mA}$
Output leakage current	I_{QLEAK}	–	–	10	μA	–
Output current limitation	I_{QLIMIT}	30	56	70	mA	internally limited and thermal shutdown
Output fall time ¹⁾	t_f	0.17	0.4	1	μs	1.2 k Ω / 50 pF, see Figure 4
Output rise time ¹⁾	t_r	0.4	0.5	1	μs	1.2 k Ω / 50 pF, see Figure 4
Output jitter ^{1) 2)}	t_{QJ}	–	0.35	1	μs	for square wave signal with 1 kHz
Delay time ^{1) 3)}	t_d	12	15	30	μs	see Figure 4
Power-on time ^{1) 4)}	t_{PON}	–	80	150	μs	$V_{DD} = 3\text{ V}$, $B \leq B_{RP} - 0.5\text{ mT}$ or $B \geq B_{OP} + 0.5\text{ mT}$
Chopper frequency ¹⁾	f_{OSC}	–	350		kHz	–

1) Not subject to production test, verified by design/characterization.

2) Output jitter is the 1 σ value of the output switching distribution.

3) Systematic delay between magnetic threshold reached and output switching.

4) Time from applying $V_{DD} = 3.0\text{ V}$ to the sensor until the output is valid.

2 Specification

Table 8 Magnetic characteristics

Parameter	Symbol	T (°C)	Values			Unit	Note or Test Condition
			Min.	Typ.	Max.		
Operating point	B_{OP}	-40	0.6	2.1	3.6	mT	–
		25	0.5	2.0	3.5		
		125	0.3	1.8	3.2		
Release point	B_{RP}	-40	-3.6	-2.1	-0.6	mT	–
		25	-3.5	-2.0	-0.5		
		125	-3.2	-1.8	-0.3		
Hysteresis	B_{HYS}	-40	2.5	4.2	5.9	mT	–
		25	2.4	4.0	5.6		
		125	2.1	3.2	5.0		
Effective noise value of the magnetic switching points ¹⁾	B_{Neff}	25	–	62	–	μT	–
Temperature compensation of magnetic thresholds ²⁾	T_C	–	–	-1200	–	ppm /K	–

- 1) The magnetic noise is normal distributed and can be assumed as nearly independent to frequency without sampling noise or digital noise effects. The typical value represents the rms-value and corresponds therefore to a 1 σ probability of normal distribution. Consequently a 3 σ value corresponds to 99.7% probability of appearance.
- 2) Not subject to production test, verified by design/characterization.

Field direction definition

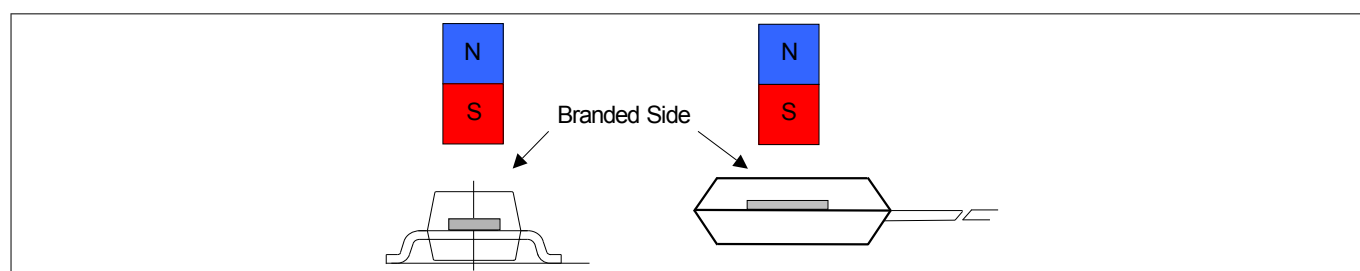


Figure 9 Definition of magnetic field direction PG-SOT23-3-15 (left hand) and PG-SSO-3-2 (right hand)

3 Package information

3 Package information

The TLI4961-1L/1M is available in the small halogen-free SMD package PG-SOT23-3-15 and the through-hole leaded package PG-SSO-3-2.

3.1 Package outline PG-SOT23-3-15

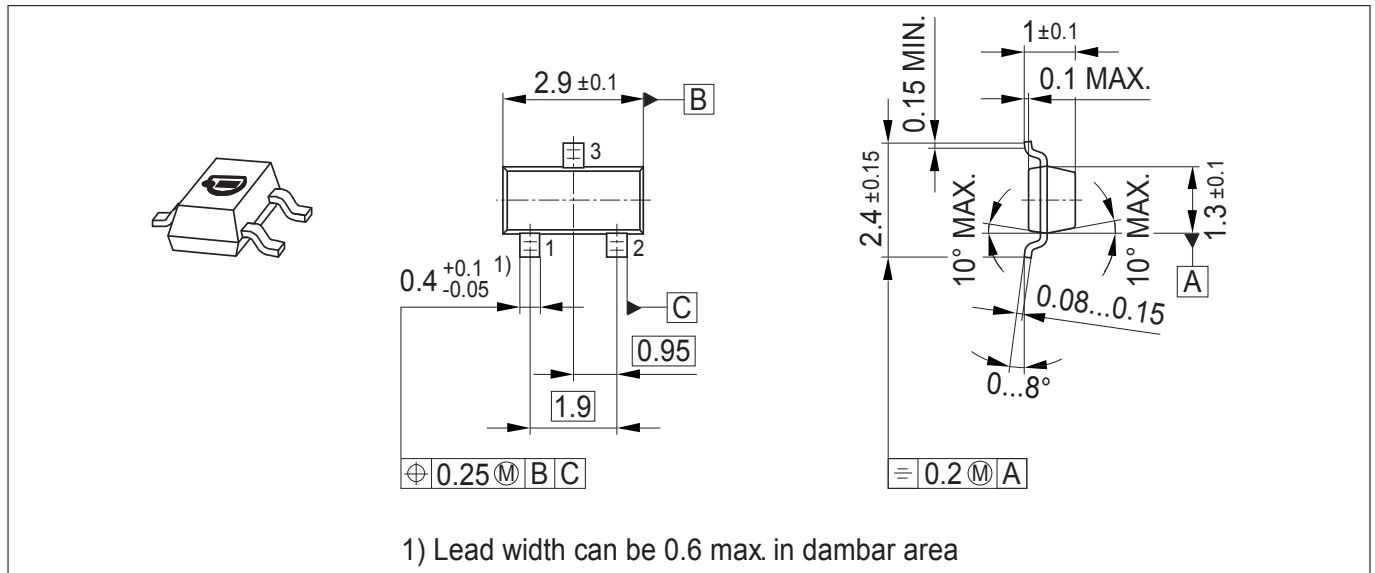


Figure 10 PG-SOT23-3-15 package outline (all dimensions in mm)

3.2 Packing information PG-SOT23-3-15

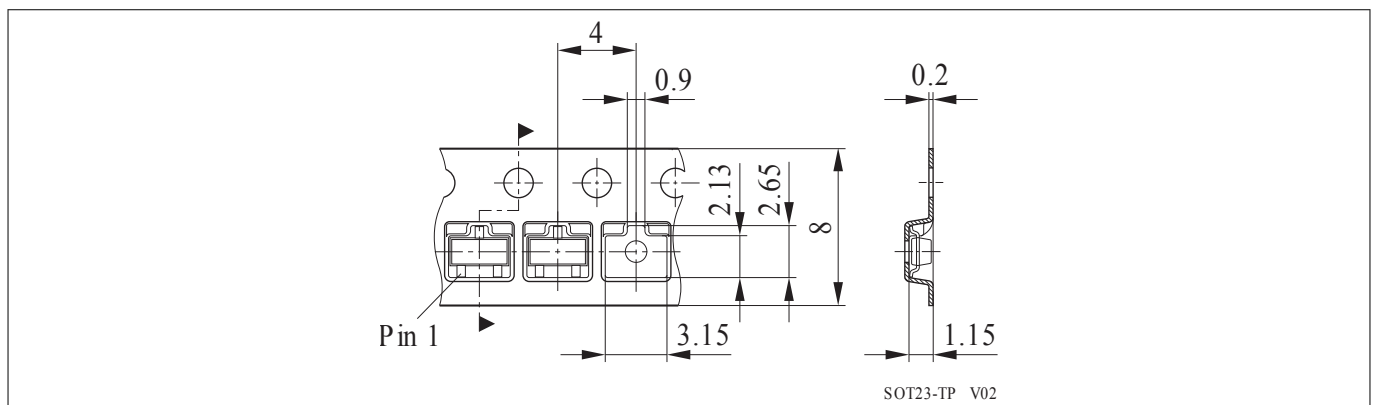


Figure 11 Packing of the PG-SOT23-3-15 in a tape

3 Package information

3.3 Package outline PG-SSO-3-2

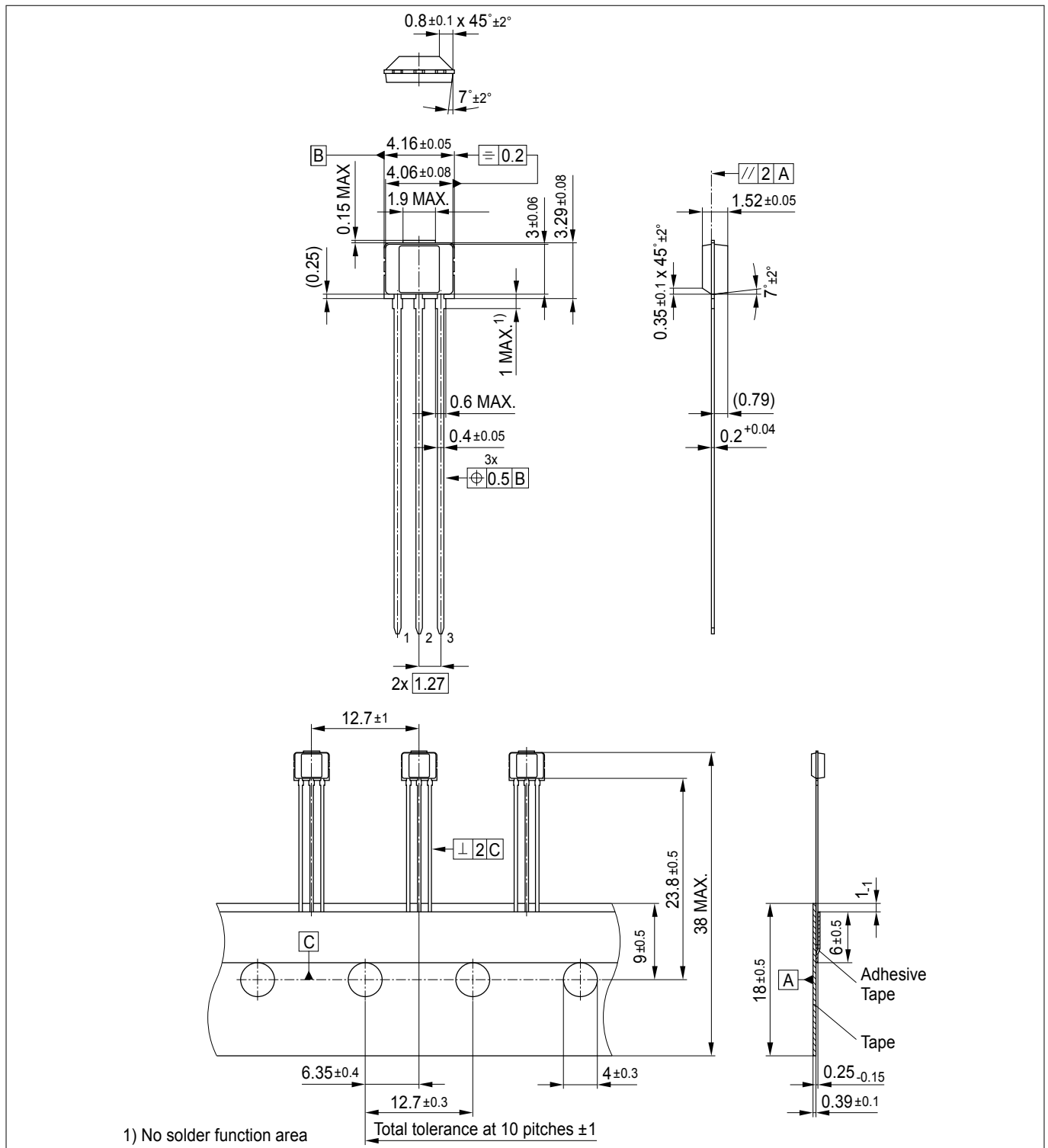


Figure 12 PG-SSO-3-2 package outline (all dimensions in mm)

3 Package information

3.4 Footprint PG-SOT23-3-15

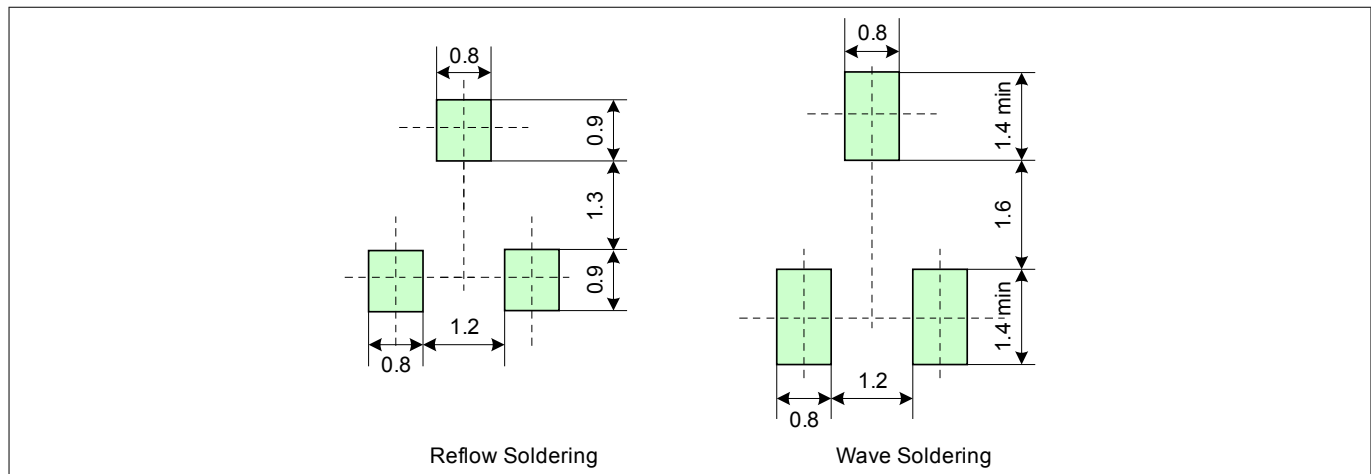


Figure 13 Footprint PG-SOT23-3-15

3.5 PG-SOT23-3-15 distance between chip and package

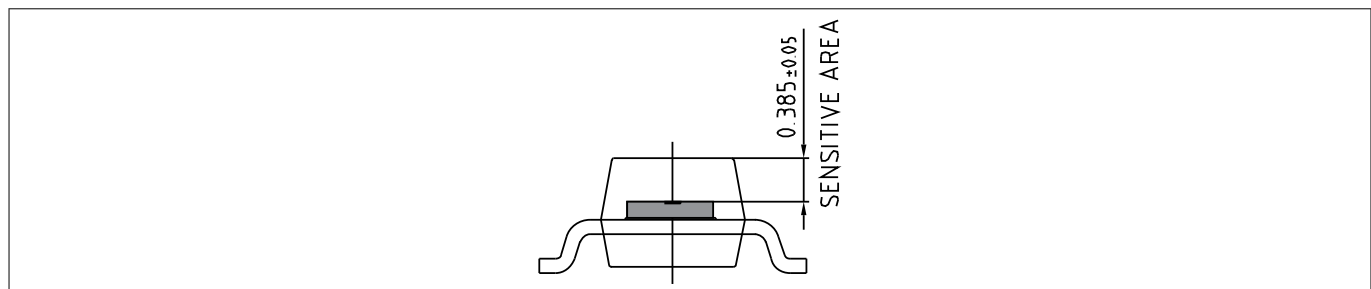


Figure 14 Distance between chip and package

3.6 PG-SSO-3-2 distance between chip and package

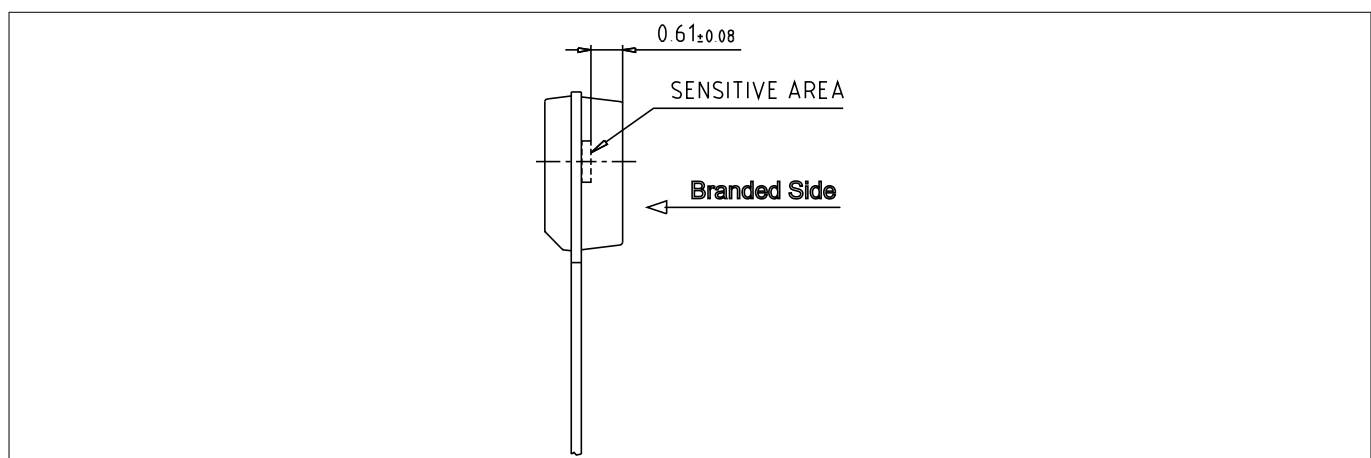


Figure 15 Distance between chip and package

3 Package information

3.7 Package marking

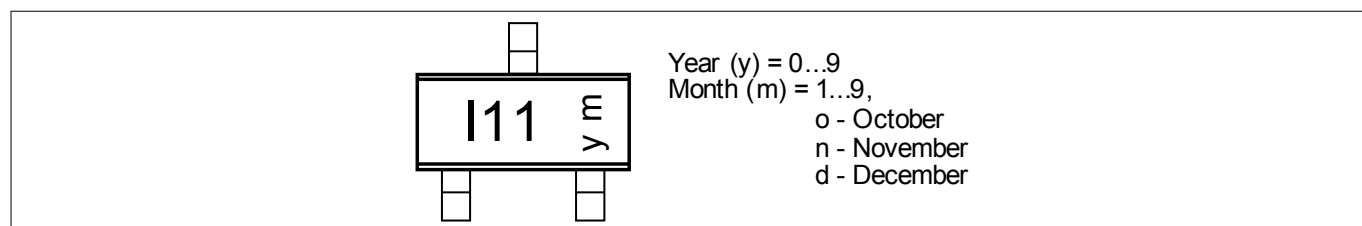


Figure 16 Marking of TLI4961-1M

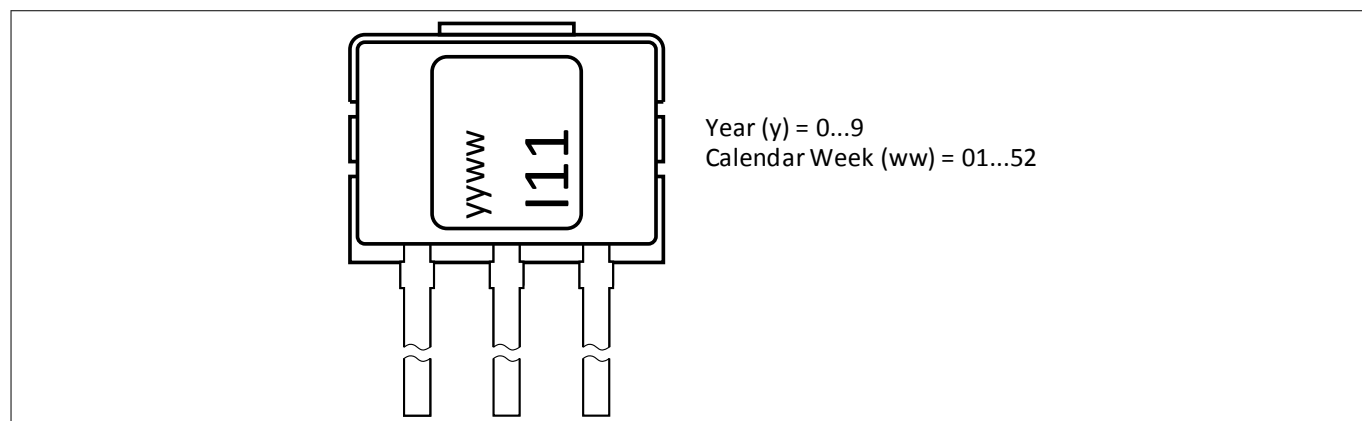


Figure 17 Marking of TLI4961-1L

Revision history

Revision history

Revision	Date	Changes
Revision 1.3	2021-05-03	Error correction of product name from TLI4964-1L/1M to TLI4961-1M
Revision 1.2	2019-12-20	• Updated text and figure in Chapter 2.6 • Updated standards in Table 5 • Added maximum tested magnetic field in Chapter 3.3 • Updated Figure 15 • Editorial changes
Revision 1.1	2012-10-15	Added TLI4961-1L with PG-SSO-3-2 package
Revision 1.0		Initial release

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2021-05-03

Published by
Infineon Technologies AG
81726 Munich, Germany

© 2021 Infineon Technologies AG
All Rights Reserved.

Do you have a question about any
aspect of this document?
Email: erratum@infineon.com

Document reference
IFX-nnt1620014101071

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenhheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Infineon:](#)

[TLI49611MXTMA1](#) [TLI4961-1M](#)