

OPTIREG™ PMIC TLF35584

Functional Safety PMIC



RoHS



ISO26262
compliant

Features

- High efficient power management integrated circuit (PMIC)
- Serial step up and step down pre regulator for wide input voltage range from 3.0 to 40 V with full performance and low over all power loss
- Low drop post regulator 5.0 V/200 mA for communication supply (QCO)
- Low drop post regulator 5.0 V/600 mA (TLF35584QxVS1) or 3.3 V/600 mA (TLF35584QxVS2) for μ C supply (QUC)
- Voltage reference 5.0 V $\pm$ 1% for ADC supply, 150 mA current capability (QVR)
- Two trackers for sensor supply following voltage reference 150 mA current capability each (QT1 and QT2)
- Standby regulator 5.0 V/10 mA (TLF35584QxVS1) or 3.3 V/10 mA (TLF35584QxVS2) (QST)
- Provides enable, sync out signal and voltage monitoring for an optional external post regulator for core supply
- Independent voltage monitoring block and error pin monitoring
- Configurable window and functional watchdog
- Safe State Control with two safe state signals with programmable delay
- 16-bit SPI, interrupt and reset function
- PRO-SIL™ Features:
 - ISO 26262 compliant supporting up to ASIL-D
 - Safety Documentation (Safety Manual & Safety Analysis Summary Report)
- Green Product (RoHS compliant)



Potential applications

- Electric Power Steering
- Battery Management
- Inverter
- Transmission
- Engine Management
- Domain Control

Product validation

Qualified for Automotive Applications.

Product validation according to AEC-Q100/101.

Description

Type	Package
TLF35584QWS1 (5.0 V Variant)	PG-VQFN-48
TLF35584QWS2 (3.3 V Variant)	PG-VQFN-48
TLF35584QKVS1 (5.0 V Variant)	PG-LQFP-64
TLF35584QKVS2 (3.3 V Variant)	PG-LQFP-64

The diagram illustrates the internal architecture and pin connections of the TLF35584 microcontroller. Key components include:

- Power Management:** LDOs for $V_{LDO_u\mu C}$ (3.3V) and V_{LDO_Com} (5.0V), a Step Up-Regulator, and a Step down-Regulator. It also features a Voltage Monitoring/Reset Function and a Safe State Control block.
- Control and Logic:** Includes a WakeUp Timer, Logic, Comparator, and Internal Supply and Clock. The device has a Reset Control block and a SMU (Safe Mode Unit).
- Communication:** Supports SPI, I2C (SCL, SDA), and CAN (FlexRay) interfaces. It also has a Trigger input and an /ErrorPin output.
- Pins and Connections:** The diagram shows various pins such as VST, ENA, WAK, V2, V1, DRG, RSH, BSG, RSL, ROT, INT, SCS, SCL, SDI, SDO, WDI, ERR, SS1, SS2, AG1, AG2, AG3, AG5, AG6, GST, QST, FRE, STU, SW1, SW2, PG1, PG2, FB1, FB2, FB3, FB4, SYN, EVC, SEC1, SEC2, QUC, SQUC, QCO, OT1, OT2, SQT1, SQT2, QVR, MPS, and AG4. It also shows connections for V_{BAT} , $V_{LDO_u\mu C}$, V_{LDO_Com} , V_{TR1} , V_{TR2} , V_{VOLT_REF} , and V_{CORE} .
- External Components:** An external switchmode post regulator (optional) is shown, which can be used for V_{CORE} supply. It includes a Sync input and a Feedback output.

The diagram is labeled with the part number **TLF35584** and includes various annotations for pin functions and internal block connections.

- Please contact us for additional supportive documentation.
- For further information you may contact <http://www.infineon.com/OPTIREG-PMIC>

Device Overview

1 Absolute maximum ratings

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Table 1 Absolute maximum ratings²⁾

$T_j = -40^{\circ}\text{C}$ to 150°C , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Voltages						
Boost driver ground	V _{BSG}	-0.3	–	0.3	V	–
Input standby LDO	V _{VST}	-0.3	–	40	V	3)4)
Input voltage pin 1 (pre regulator)	V _{VS1}	-0.3	–	40	V	–
Input voltage pin 2 (pre regulator)	V _{VS2}	-0.3	–	40	V	PG-LQFP-64 only
External step up power stage, gate	V _{DRG}	-0.3	–	40	V	–
External power stage, sense resistor high	V _{RSH}	-0.3	–	40	V	–
External power stage, sense resistor low	V _{RSL}	-0.3	–	6.0	V	–
Enable input	V _{ENA}	-0.3	–	40	V	–
Enable input	I _{ENA}	-5	–	–	mA	5)
Wake input	V _{WAK}	-0.3	–	40	V	–
Wake input	I _{WAK}	-5	–	–	mA	–
Reset output	V _{ROT}	-0.3	–	6.0	V	–
SPI chip select input	V _{SCS}	-0.3	–	6.0	V	–
SPI clock input	V _{SCL}	-0.3	–	6.0	V	–
SPI data in (MOSI) input	V _{SDI}	-0.3	–	6.0	V	–
SPI data out (MISO output)	V _{SDO}	-0.3	–	6.0	V	–
Interrupt output	V _{INT}	-0.3	–	6.0	V	–
Window watchdog trigger input	V _{WDI}	-0.3	–	6.0	V	–
Error pin input	V _{ERR}	-0.3	–	6.0	V	–
Safe state 1 output	V _{SS1}	-0.3	–	6.0	V	–
Safe state 2 output	V _{SS2}	-0.3	–	6.0	V	–
Output voltage reference LDO	V _{QVR}	-0.3	–	6.0	V	–
Output tracker 2	V _{QT2}	-1.0	–	40	V	–

²⁾ Not subject to production test, specified by design.

³⁾ Maximum rating is 60 V, if rise time from 0 to 60 V is longer than 10 ms

⁴⁾ Maximum rating is 49 V, for an overall time of 10 s (in the range of 40 V to 49 V) during the lifetime of the product independent from the rise time.

⁵⁾ Consider external series resistor for negative voltages < -0.3 V to ensure maximum rating of current

1 Absolute maximum ratings

Table 1 Absolute maximum ratings²⁾ (continued)

$T_j = -40^{\circ}\text{C}$ to 150°C , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Sense Pin for tracker 2	V_{SQT2}	-0.3	–	40	V	PG-LQFP-64 only
Output tracker 1	V_{QT1}	-1.0	–	40	V	–
Sense Pin for tracker 1	V_{SQT1}	-0.3	–	40	V	PG-LQFP-64 only
Output communication LDO	V_{QCO}	-0.3	–	6.0	V	–
Output microcontroller LDO	V_{QUC}	-0.3	–	6.0	V	–
Sense Pin for microcontroller LDO	V_{SQUC}	-0.3	–	6.0	V	PG-LQFP-64 only
External core voltage monitor input	V_{VCI}	-0.3	–	6.0	V	–
HW config: ext. core voltage monitor	V_{SEC}	-0.3	–	6.0	V	–
Synchronization output	V_{SYN}	-0.3	–	6.0	V	–
Enable output for ext. core supply	V_{EVC}	-0.3	–	6.0	V	–
Step down feedback input 4	V_{FB4}	-0.3	–	7.0	V	PG-LQFP-64 only
Step down feedback input 3	V_{FB3}	-0.3	–	7.0	V	PG-LQFP-64 only
Step down feedback input 2	V_{FB2}	-0.3	–	7.0	V	–
Step down feedback input 1	V_{FB1}	-0.3	–	7.0	V	–
Step down power ground 2	V_{PG2}	-0.3	–	0.3	V	–
Step down power ground 1	V_{PG1}	-0.3	–	0.3	V	–
Step down switching node 2	V_{SW2}	-0.3	–	40	V	PG-LQFP-64 only
Step down switching node 1	V_{SW1}	-0.3	–	40	V	–
HW config: step up pre regulator	V_{STU}	-0.3	–	6.0	V	–
HW config: step down frequency	V_{FRE}	-0.3	–	6.0	V	–
Output standby LDO	V_{QST}	-0.3	–	6.0	V	–
Input MPS	V_{MPS}	-0.3	–	6.0	V	–

Temperatures

Junction temperature	T_j	-40	–	150	$^{\circ}\text{C}$	–
Storage temperature	T_{stg}	-55	–	150	$^{\circ}\text{C}$	–

ESD susceptibility

ESD susceptibility to GND	V_{ESD}	-2	–	2	kV	HBM ⁶⁾
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²⁾ Not subject to production test, specified by design.

⁶⁾ ESD susceptibility, HBM according to JEDEC HBM Human Body Model ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

1 Absolute maximum ratings

Table 1 Absolute maximum ratings²⁾ (continued)

$T_j = -40^{\circ}\text{C}$ to 150°C , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ESD susceptibility to GND	V_{ESD}	-500	–	500	V	CDM ⁷⁾
ESD susceptibility (corner pins) to GND	$V_{\text{ESD,Corner}}$	-750	–	750	V	CDM

²⁾ Not subject to production test, specified by design.

⁷⁾ ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1

2 Package information ⁸⁾

⁸⁾ Dimensions in mm

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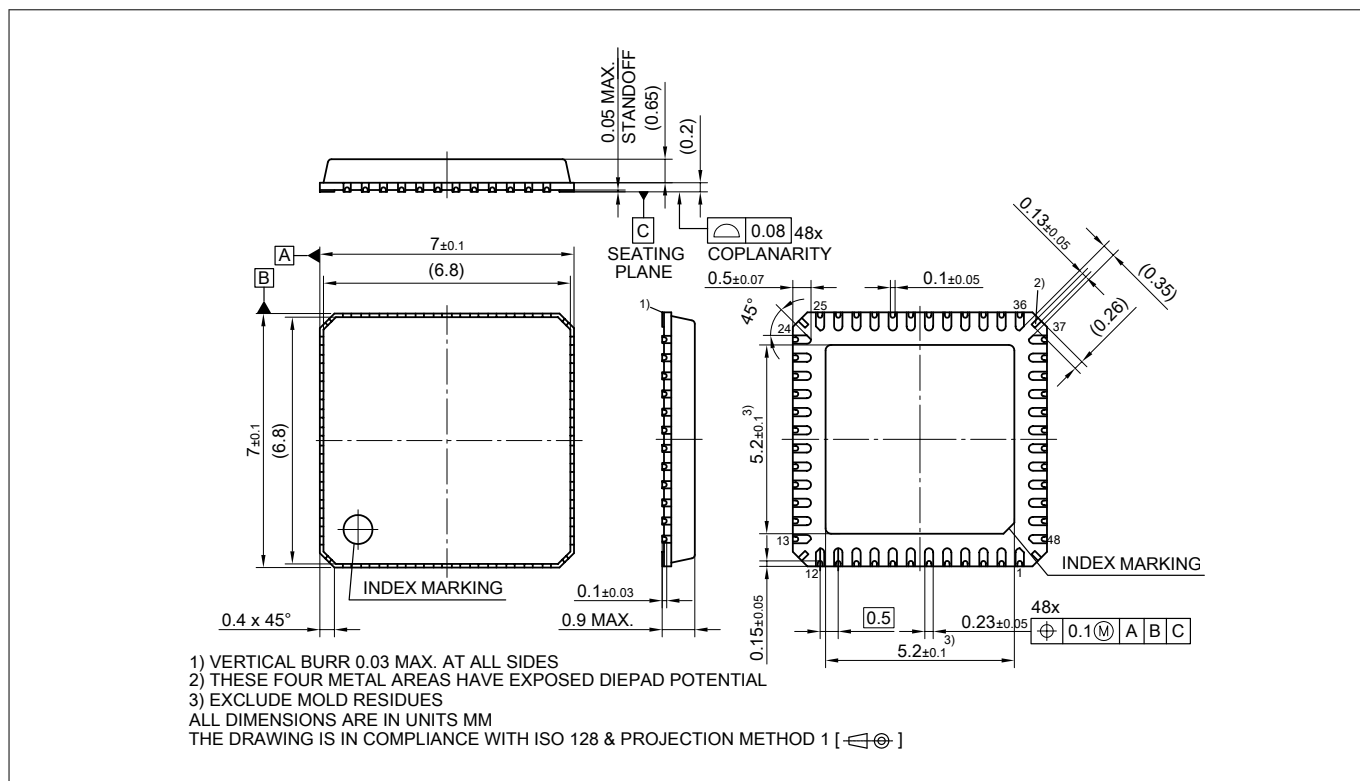


Figure 1 PG-VQFN-48 package outline

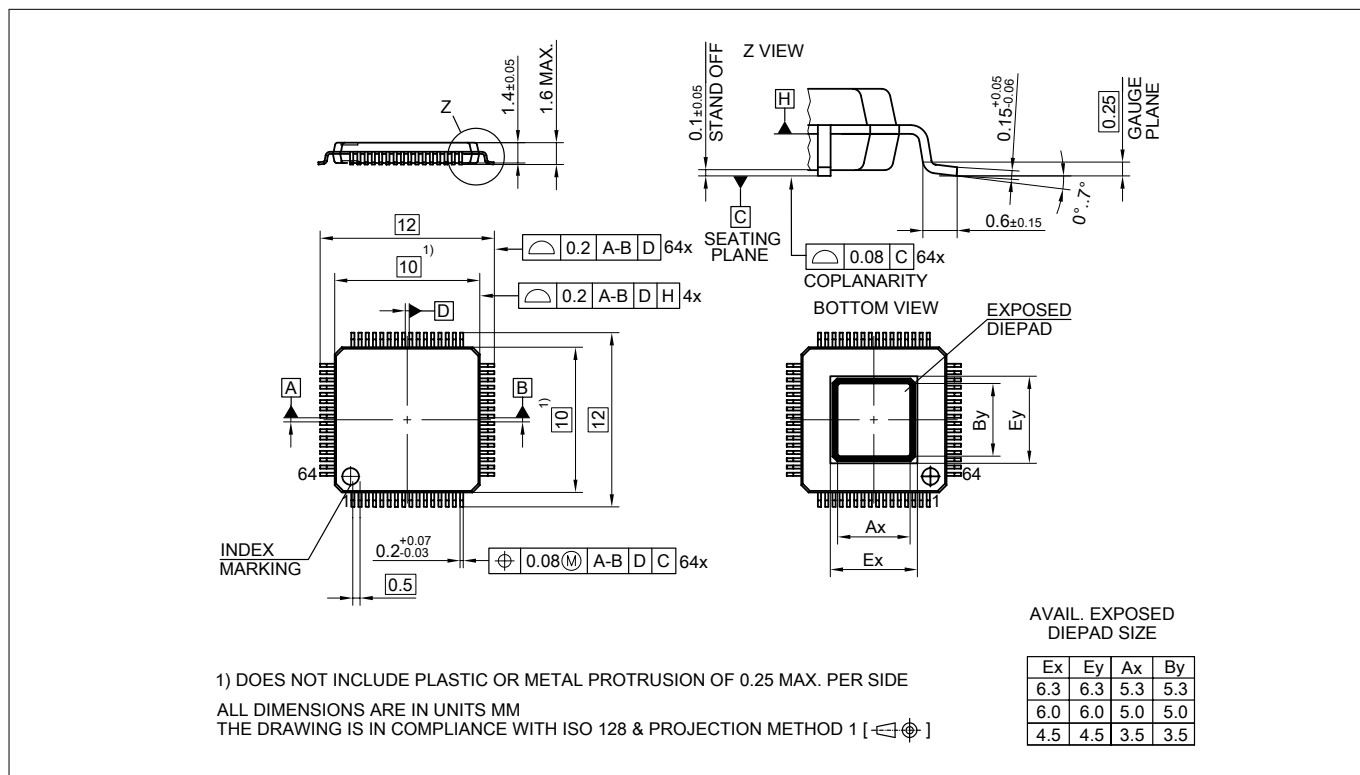


Figure 2 PG-LQFP-64 package outline

⁸⁾ Dimensions in mm

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Edition 2019-03-25

Published by
Infineon Technologies AG
81726 Munich, Germany

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Document reference
IFX-jmv1546509847065

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