

AURIX™ TC2xx Data Sheet Addendum

About this document

Scope and purpose

This is an addendum to the TC2xx Data Sheet listing all intended product variants, key parameters such as memory size, and optional features.

Prefix naming conventions

- SAK: T_{ambient} Temperature Range from -40 °C up to +125 °C
- SAL: T_{ambient} Temperature Range from -40 °C up to +150 °C (packaged device)

Feature package naming conventions

- T – Standard type without HSM
- TP – Standard type with HSM enabled
- TA – ADAS feature package – HSM enabled
- TX – Truck / SRAM extension – HSM enabled

Table of contents

About this document.....	1
Table of contents.....	1
1 TC21x.....	2
2 TC22x.....	3
3 TC23x.....	4
3.1 Standard variants TC23x.....	4
3.2 ADAS type TC23x.....	4
3.3 Extended type TC23x.....	4
4 TC26x.....	5
4.1 Standard variants TC26x.....	5
4.2 ADAS type TC26x.....	5
5 TC27x.....	6
6 TC29x.....	7
6.1 Standard variants TC29x.....	7
6.2 Extended type TC29x.....	7
6.3 ADAS Type TC29x.....	7
7 Memory map of variants	8
7.1 TC21x	8
7.2 TC22X	9
7.3 TC23x	10
7.4 TC26x	14
7.5 TC27x	18
7.6 TC29x	21
Revision history.....	28

TC21x

1 TC21x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 0 TC16E		ADC CHAN.	FlexRay (#/ch.)	ETH	HSM	LOCK-STEP	CAN FD	CAN FD ISO 11898-1
									DSPR (KB)	PSPR (KB)							
SAK-TC214L-8F133N AC	STANDARD	PG-TQFP-144-27	-40°C - +125 °C	0146 1142 _H	133	0.5	64@125k	56	48	8	24	No	No	No	Yes	Yes	Yes
SAK-TC213L-8F133N AC	STANDARD	PG-TQFP-100-23	-40°C - +125 °C	0146 1042 _H	133	0.5	64@125k	56	48	8	24	No	No	No	Yes	Yes	Yes
SAK-TC213L-8F133F AC	STANDARD	PG-TQFP-100-23	-40°C - +125 °C	0146 1042 _H	133	0.5	64@125k	56	48	8	24	No	No	No	Yes	Yes	No
SAK-TC212L-8F133F AC	STANDARD	PG-TQFP-80-7	-40°C - +125 °C	0146 1242 _H	133	0.5	64@125k	56	48	8	14	No	No	No	Yes	Yes	No
SAK-TC212L-8F133N AC	STANDARD	PG-TQFP-80-7	-40°C - +125 °C	0146 1242 _H	133	0.5	64@125k	56	48	8	14	No	No	No	Yes	Yes	Yes

TC22x

2 TC22x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 0 TC16E		ADC Chan.	FlexRay (#/ch.)	ETH	HSM	LOCK STEP	CAN FD	CAN FD
									DSPR (KB)	PSPR (KB)							
SAK-TC224L-16F133N AC	STANDARD	PG-TQFP-144-27	-40°C - +125 °C	0246 2142 _H	133	1	96@ 125k	96	88	8	24	No	No	No	Yes	Yes	Yes
SAK-TC223L-16F133N AC	STANDARD	PG-TQFP-100-23	-40°C - +125 °C	0246 2042 _H	133	1	96@125k	96	88	8	24	No	No	No	Yes	Yes	Yes
SAK-TC222L-16F133N AC	STANDARD	PG-TQFP-80-7	-40°C - +125 °C	0246 2242 _H	133	1	96@125k	96	88	8	14	No	No	No	Yes	Yes	Yes

TC23x

3 TC23x

3.1 Standard variants TC23x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 0 TC16E		ADC Chan.	FlexRay (#/ch.)	ETH	HSM	CAN FD
									DSPR (KB)	PSPR (KB)					ISO 11898-1
SAK-TC237LP-32F200N AC	STANDARD	PG-LFBGA-292-6	-40°C - +125 °C	4446 3242 _H	200	2	128@125k	192	184	8	24	1 / 2	No	Yes	Yes
SAK-TC234LP-32F200N AC	STANDARD	PG-TQFP-144-27	-40°C - +125 °C	4446 3142 _H	200	2	128@125k	192	184	8	24	1 / 2	No	Yes	Yes
SAK-TC233LP-32F200N AC	STANDARD	PG-TQFP-100-23	-40°C - +125 °C	4446 3042 _H	200	2	128@125k	192	184	8	24	1 / 2	No	Yes	Yes

3.2 ADAS type TC23x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 0 TC16E		LMU (KB)	EMEM (KB)	ADC Chan.	FlexRay (#/ch.)	ETH	HSM	FFT
									DSPR (KB)	PSPR (KB)							
SAK-TC234LA-32F200F AB	STANDARD	PG-TQFP-144-27	-40°C - +125 °C	4443 3941 _H 4447 3941 _H	200	2	128@125k	736	184	8	32	512	24	1 / 2	Yes	Yes	Yes

3.3 Extended type TC23x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 0 TC16E		LMU (KB)	EMEM (KB)	ADC Chan.	FlexRay (#/ch.)	ETH	HSM	FFT
									DSPR (KB)	PSPR (KB)							
SAK-TC234LX-32F200F AB	STANDARD	PG-TQFP-144-27	-40°C - +125 °C	4443 3941 _H 4447 3941 _H	200	2	128@125k	736	184	8	32	512	24	1 / 2	Yes	Yes	No

TC26x

4 TC26x

4.1 Standard variants TC26x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 1 TC16P		CORE 0 TC16E		LMU (KB)	ADC CHAN.	ETH	CAN FD	CAN FD ISO frame
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)					
SAK-TC267D-40F200N BC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	0546 6652 _H	200	2.5	16 @500k	240	120	32	72	16	0	50	Yes	Yes	Yes
SAK-TC267D-40F200S BC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	0544 6651 _H	200	2.5	16 @500k	240	120	32	72	16	0	50	Yes	Yes	No
SAK-TC265D-40F200N BC	STANDARD	PG-LQFP-176-22	-40°C – +125°C	0546 6152 _H	200	2.5	16 @500k	240	120	32	72	16	0	50	Yes	Yes	Yes
SAK-TC264D-40F200N BC	STANDARD	PG-LQFP-144-22	-40°C – +125°C	0546 6052 _H	200	2.5	16 @500k	240	120	32	72	16	0	40	Yes	Yes	Yes
SAL-TC267D-40F200N BC	STANDARD	PG-LFBGA-292-6	-40°C – +150°C	0546 6652 _H	200	2.5	16 @500k	240	120	32	72	16	0	50	Yes	Yes	Yes

4.2 ADAS type TC26x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 1 TC16P		CORE 0 TC16E		LMU (KB)	EMEM (KB)	ADC CHAN.	ETH	CIF	FFT	CAN FD	CAN FD ISO frame
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)								
SAK-TC264DA-40F200N BC	STANDARD	PG-LQFP-144-22	-40°C – +125°C	0547 6852 _H	200	2.5	16 @500k	752	120	32	72	16	0	512	40	Yes	Yes	Yes	Yes	Yes

TC27x

5 TC27x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 1 AND 2 TC16P		CORE 0 TC16E		LMU (KB)	ADC CHAN.	FlexRay (#/ch.)	ETH	HSM	CAN FD	CAN FD
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)							ISO frame
SAK-TC277TP-64F200N DC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	4746 7172 _H	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	Yes	Yes	Yes
SAK-TC277TP-64F200S DC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	4746 7172 _H	200	4	64 @ 500k	472	120	32	112	24	32	60	1 / 2	Yes	Yes	Yes	No
SAK-TC275TP-64F200N DC	STANDARD	PG-LQFP-176-22	-40°C – +125°C	4746 7072 _H	200	4	64 @ 500k	472	120	32	112	24	32	48	1 / 2	Yes	Yes	Yes	Yes

TC29x

6 TC29x

6.1 Standard variants TC29x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMPERATURE RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 1 AND 2 TC16P		CORE 0 TC16P		LMU (KB)	ADC CHAN.	FlexRay (#/ch.)	ETH	HSM	CAN FD	CAN FD ISO frame
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)							
SAL-TC299TP-128F300N BC	STANDARD	PG-LFBGA-516-5	-40°C – +150°C	4B46 9252 _H	300	8	128@500k	728	240	32	120	32	32	84	2 / 4	Yes	Yes	Yes	Yes
SAL-TC298TP-128F300N BC	STANDARD	PG-LBGA-416-26	-40°C – +150°C	4B46 9152 _H	300	8	128@500k	728	240	32	120	32	32	60	2 / 4	Yes	Yes	Yes	Yes
SAK-TC297TP-128F300N BC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	4B46 9052 _H	300	8	128@500k	728	240	32	120	32	32	60	2 / 4	Yes	Yes	Yes	Yes

6.2 Extended type TC29x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMP. RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 1 AND 2 TC16P		CORE 0 TC16P		LMU (KB)	EMEM (KB)	ADC CHAN.	FlexRay (#/ch.)	ETH	CIF	FFT	HSM	CAN FD	CAN FD ISO frame	AGBT
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)											
SAK-TC299TX-128F300N BC	STANDARD	PG-LFBGA-516-5	-40°C – +125°C	4B47 9A52 _H	300	8	128 @500k	2776	240	32	120	32	32	2048	84	2 / 4	Yes	No	No	Yes	Yes	Yes	No
SAK-TC297TX-128F300N BC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	4B47 9852 _H	300	8	128 @500k	2776	240	32	120	32	32	2048	60	2 / 4	Yes	No	No	Yes	Yes	Yes	No

6.3 ADAS Type TC29x

DERIVATIVE	PRODUCTION STATUS	PACKAGE TYPE	TEMP. RANGE	CHIP ID	FREQ. (MHz)	FLASH (MB)	EEPROM (KB)	TOTAL SRAM (KB)	CORE 1 AND 2 TC16P		CORE 0 TC16P		LMU (KB)	EMEM (KB)	ADC Chan	Flex Ray (#/ch.)	ETH	CIF	FFT	HSM	CAN FD	CAN FD ISO frame	AGBT
									DSPR (KB)	PSPR (KB)	DSPR (KB)	PSPR (KB)											
SAK-TC297TA-128F300N BC	STANDARD	PG-LFBGA-292-6	-40°C – +125°C	4B47 9052 _H	300	8	128 @500k	2776	240	32	120	32	32	2048	60	2 / 4	Yes	Yes	Yes	Yes	Yes	Yes	No

Memory map of variants

7 Memory map of variants

This section shows the influence of the feature variants on the memory map.

7.1 TC21x

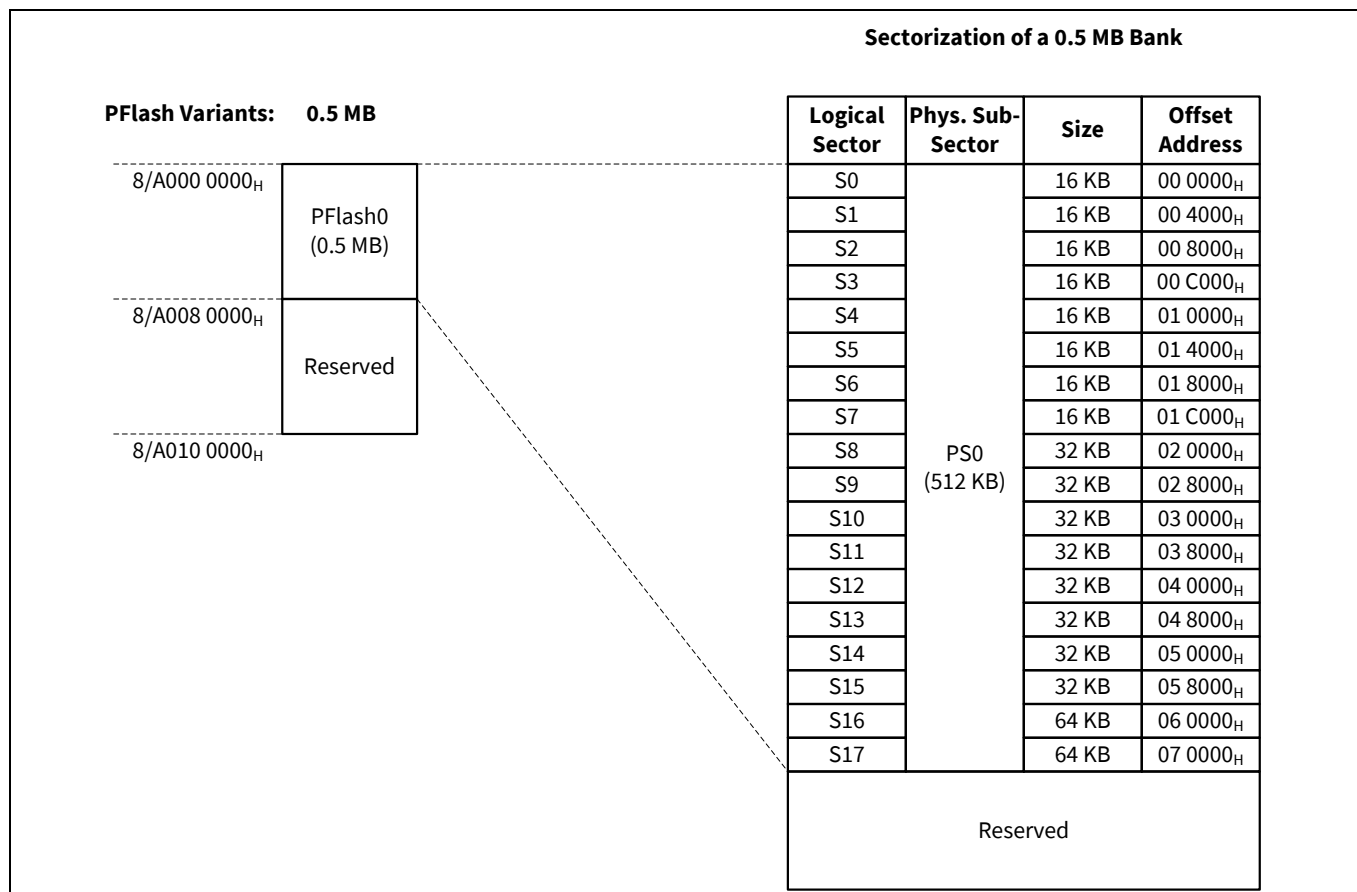


Figure 1 TC21x PFlash variants

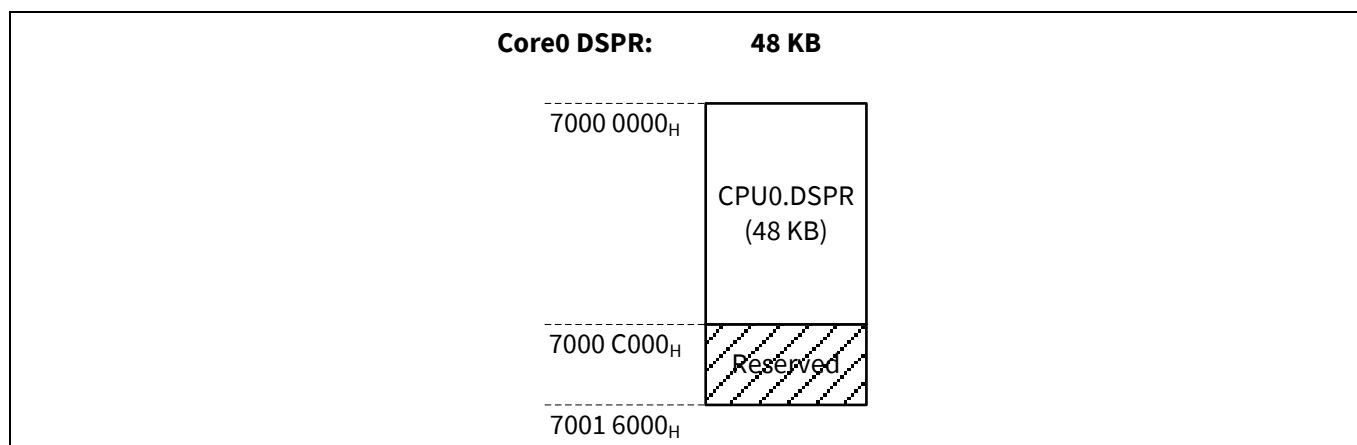


Figure 2 TC21x Coar0 DSPR

Lockstep Variants

No influence on memory ap.

Lockstep = “No” variants: In the Boot Mode Header the BMI.LCL0LSEN must be configured to 0_B.

Memory map of variants

7.2 TC22X

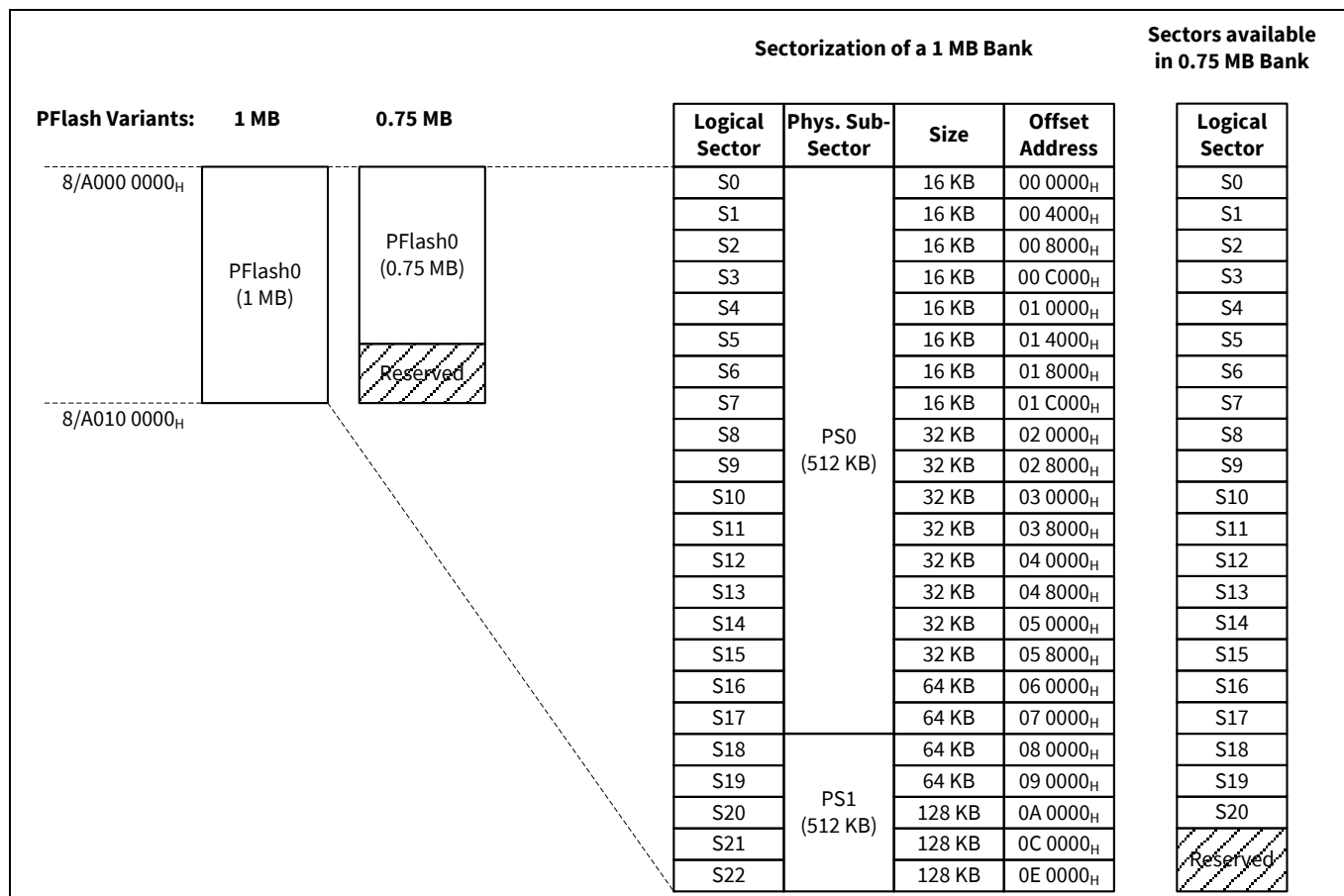


Figure 3 TC22x PFlash variants

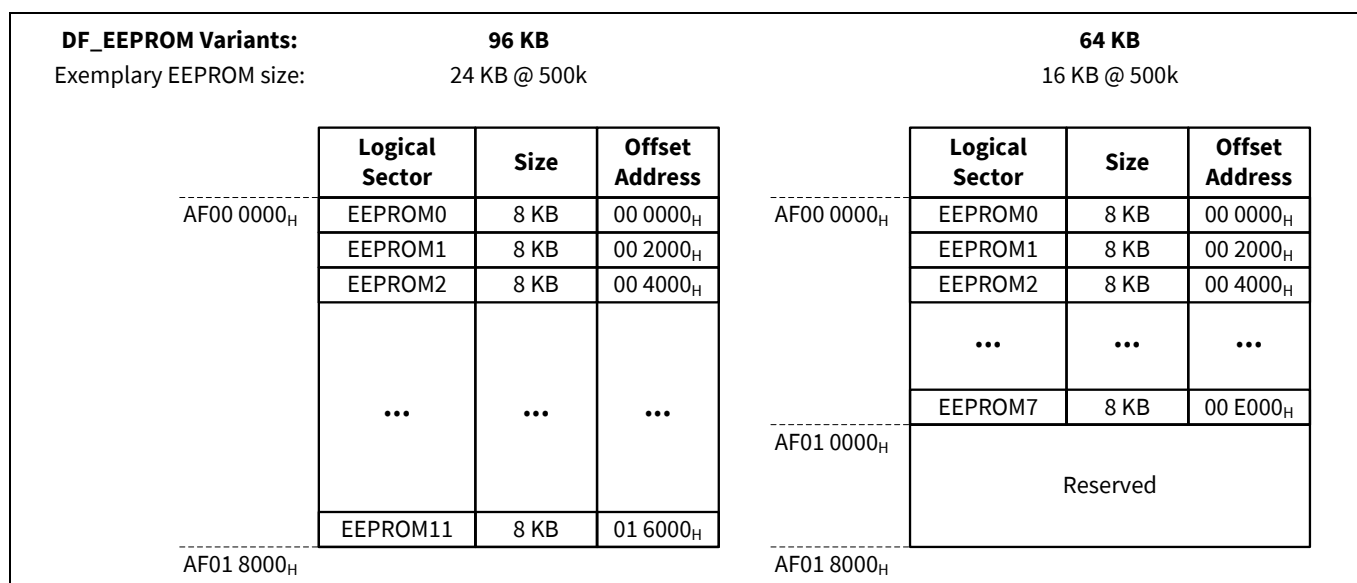


Figure 4 TC22x DF_EEPROM variants

Memory map of variants

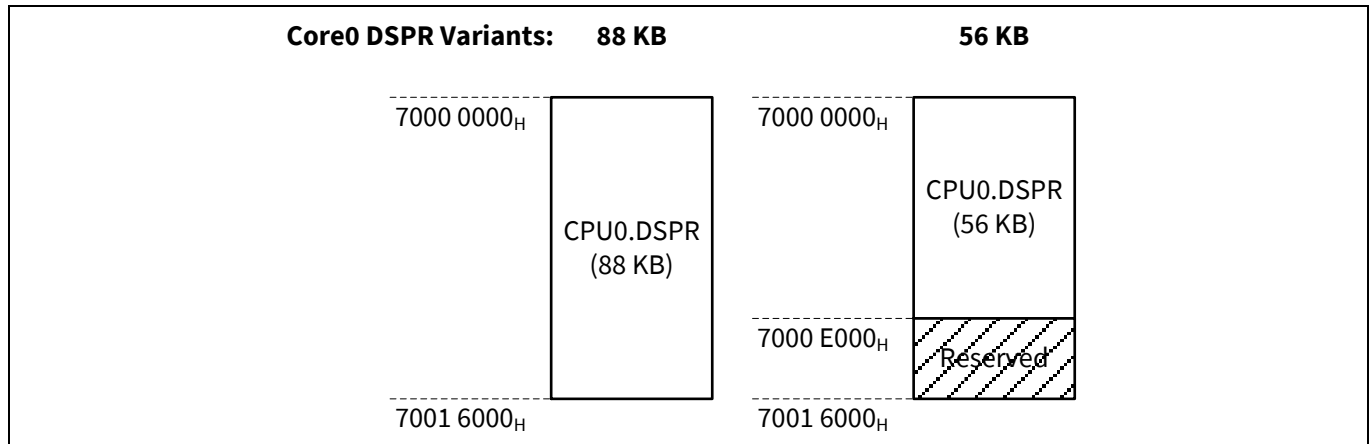


Figure 5 TC22x Core0 DSPR variants

7.3 TC23x

Sectorization of a 2 MB Bank				Sectors available in 1.5 MB Bank	Sectors available in 1 MB Bank
PFlash Variants:	2 MB	1.5 MB	1 MB	Logical Sector	Logical Sector
8/A000 0000 _H	PFlash0 (2 MB)	PFlash0 (1.5 MB)	PFlash0 (1 MB)	S0	S0
				S1	S1
				S2	S2
				S3	S3
				S4	S4
				S5	S5
				S6	S6
				S7	S7
				S8	S8
				S9	S9
				S10	S10
				S11	S11
				S12	S12
				S13	S13
				S14	S14
				S15	S15
				S16	S16
				S17	S17
				S18	S18
				S19	S19
				S20	S20
				S21	S21
				S22	S22
				S23	Reserved
				S24	
				S25	
				S26	
8/A020 0000 _H		Reserved	Reserved	Reserved	

Figure 6 TC23x PFlash variants

Memory map of variants

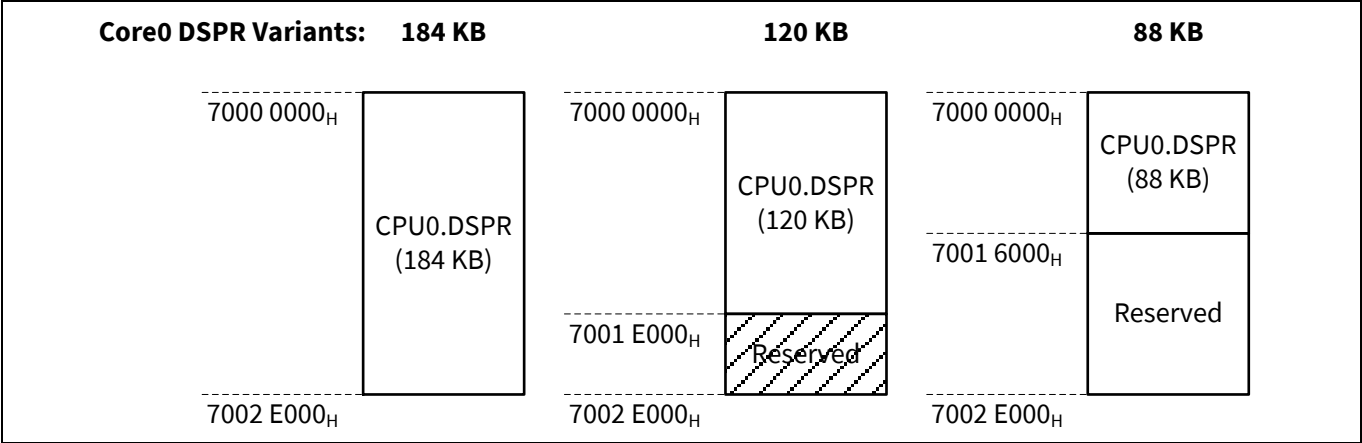


Figure 7 TC23x Core0 DSPR variants

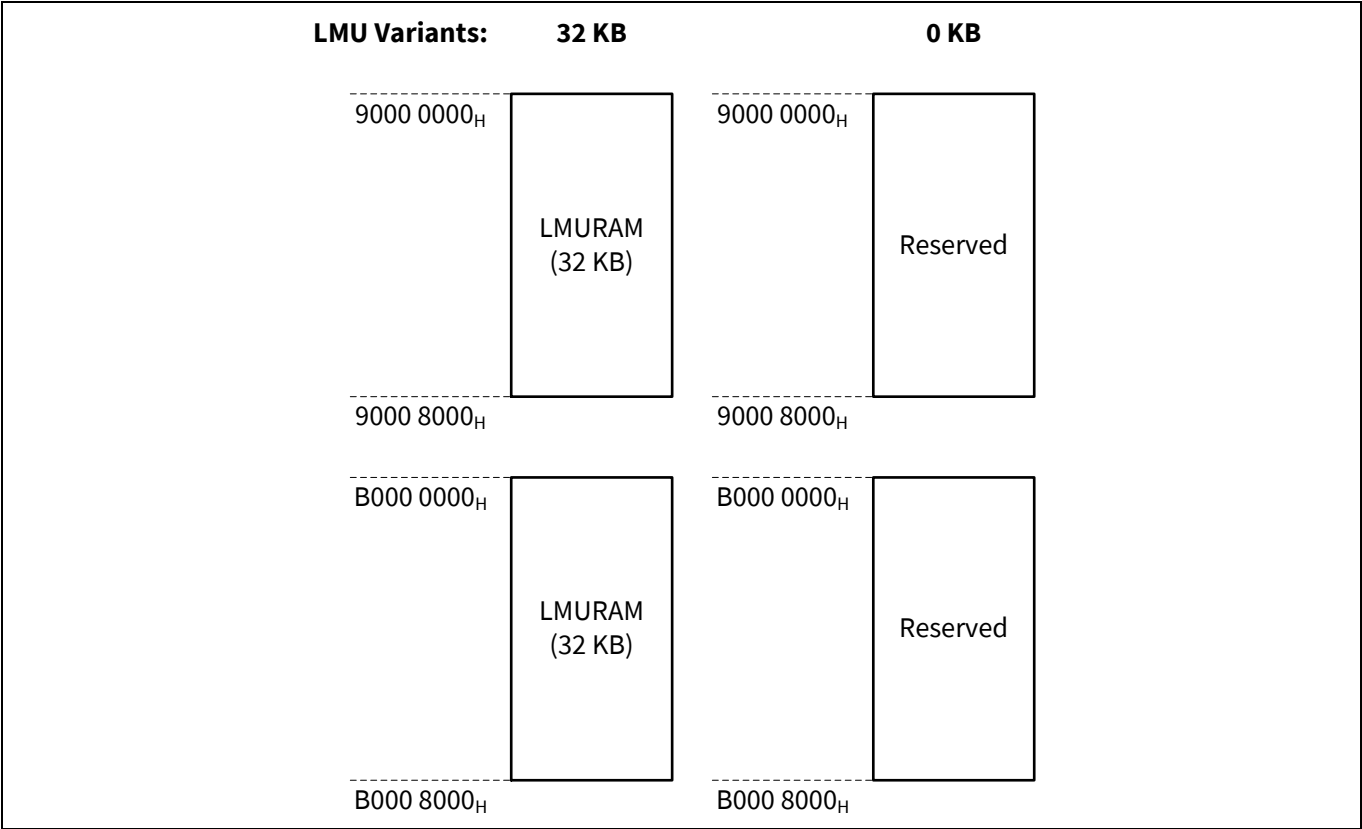


Figure 8 TC23x LMU variants

Memory map of variants

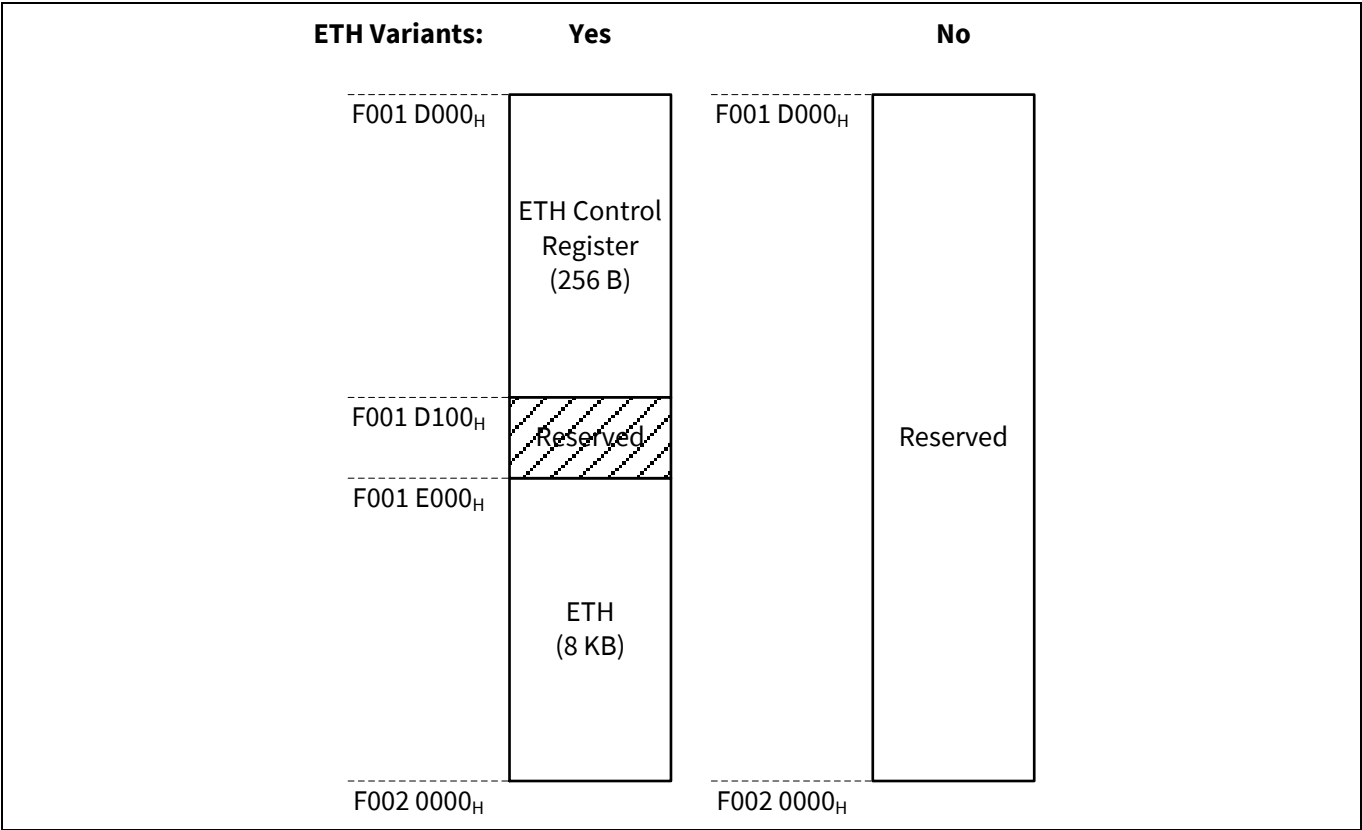


Figure 9 TC23x ETH variants

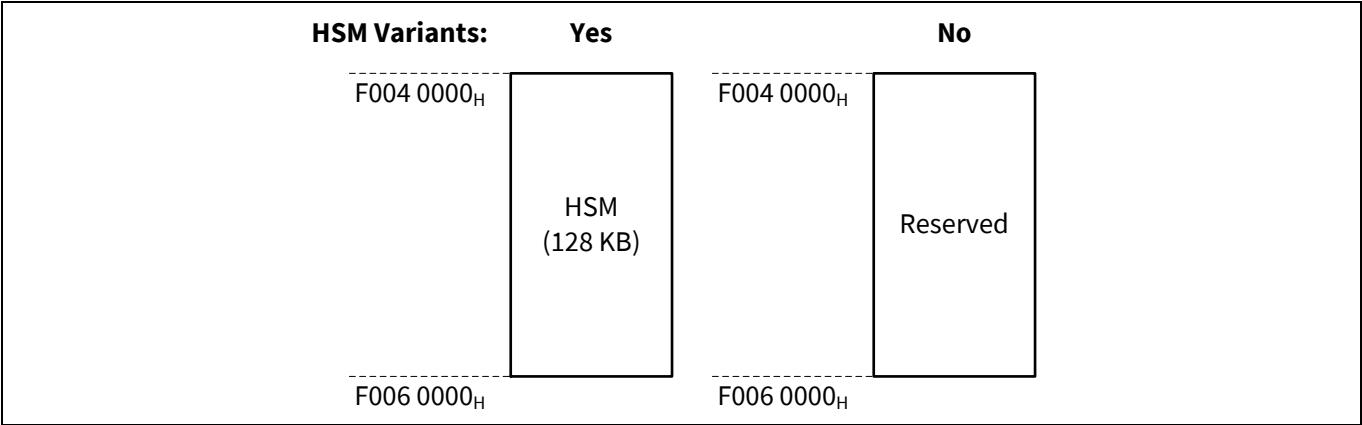


Figure 10 TC23x HSM variants

Memory map of variants

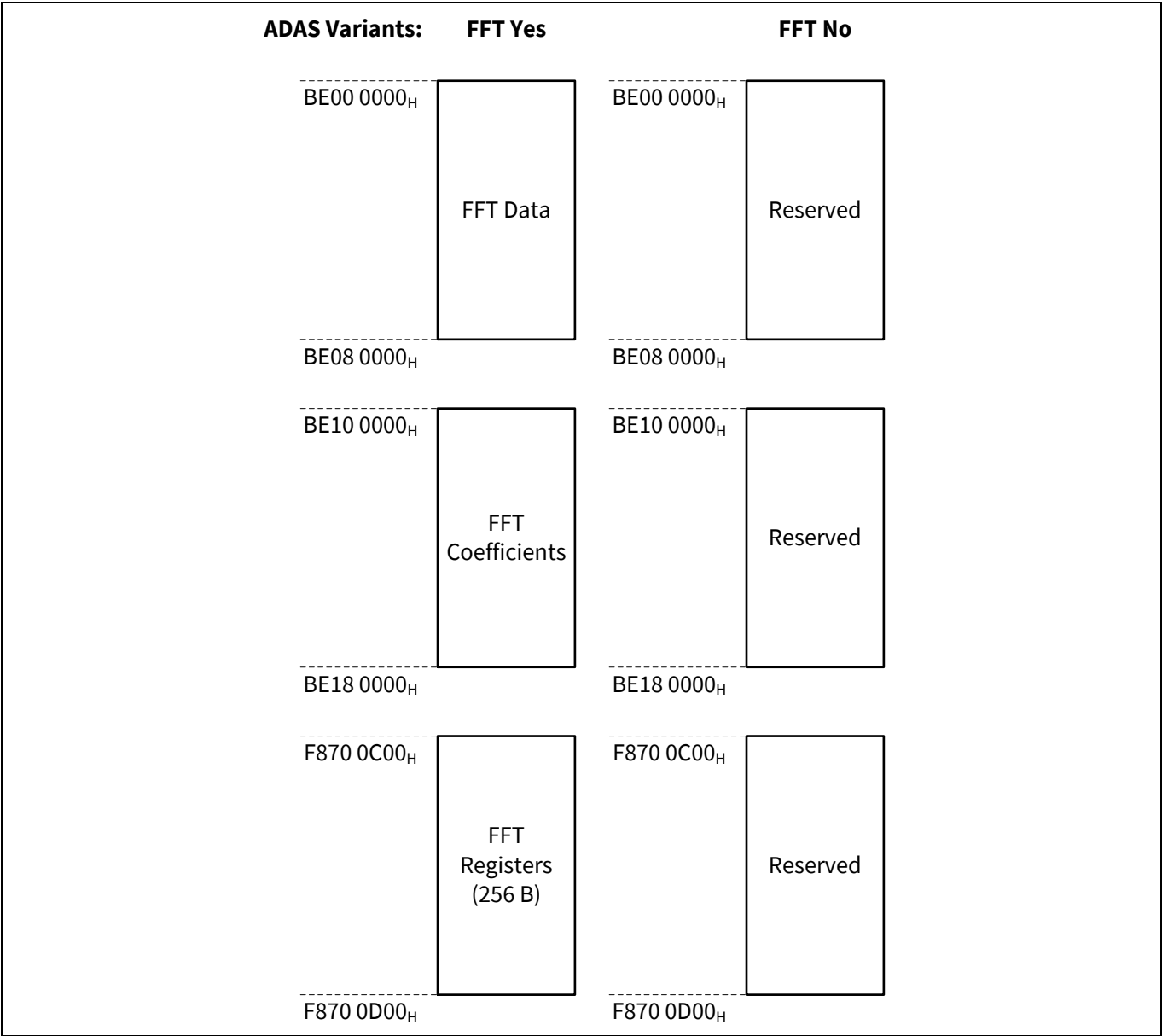


Figure 11 TC23x ADAS variants

ADAS variants

ADAS = “Yes” variants:

The VADC kernels ADC02 and ADC03 are available, offering the Converter Groups G02 and G03. Because of that, the group related registers with x = 2 and x = 3 are implemented.

Memory map of variants

7.4 TC26x

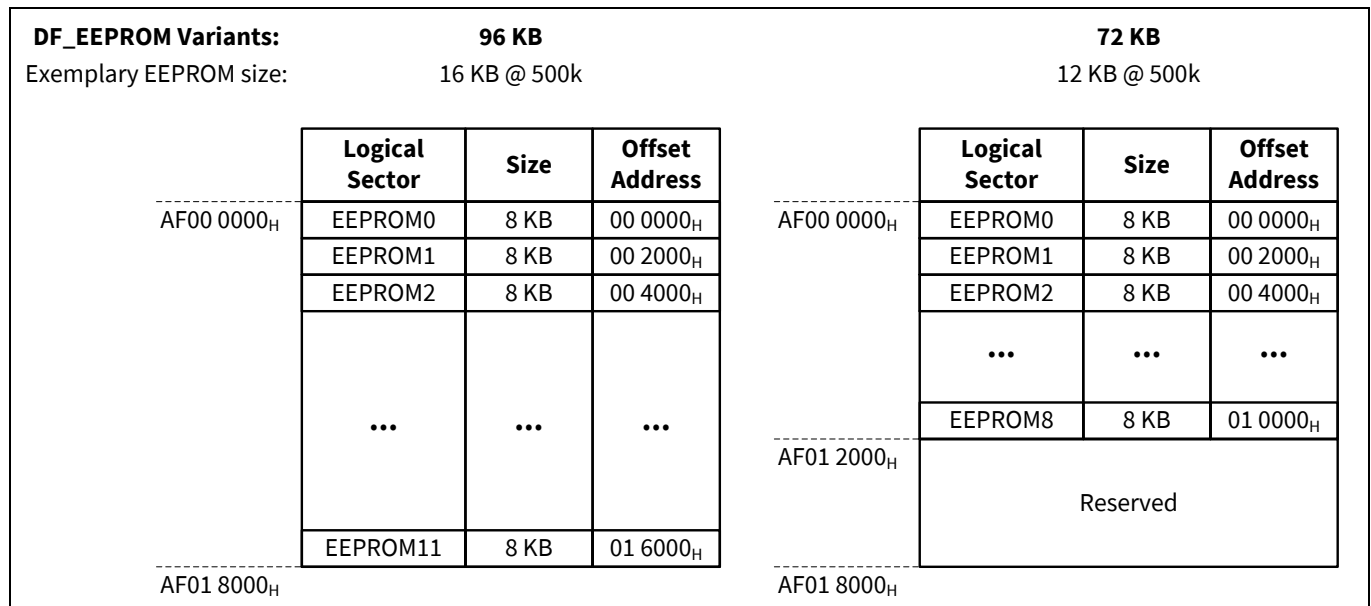


Figure 12 TC26x DF_EEPROM variants

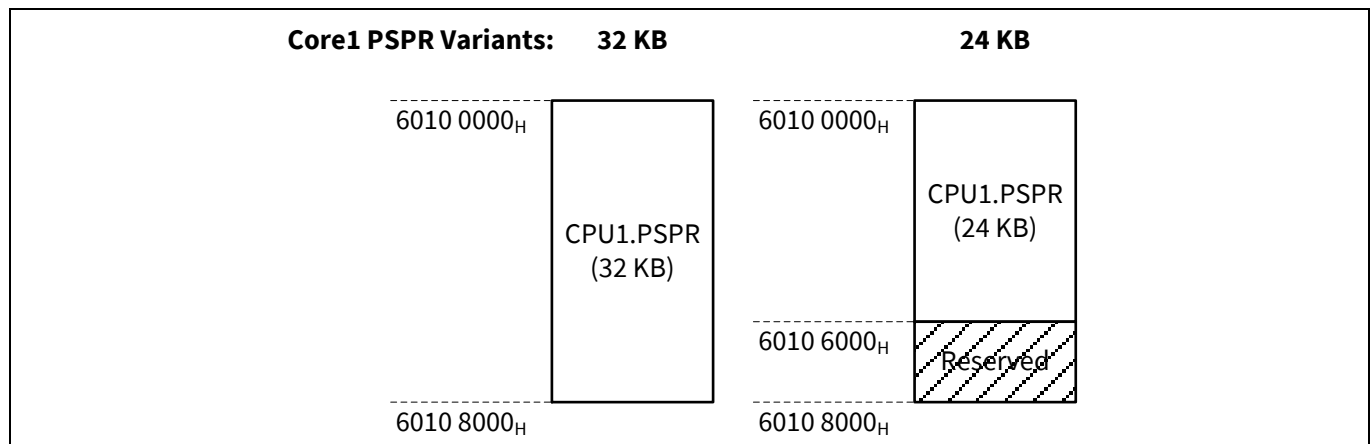


Figure 13 TC26x Core1 PSPR variants

Memory map of variants

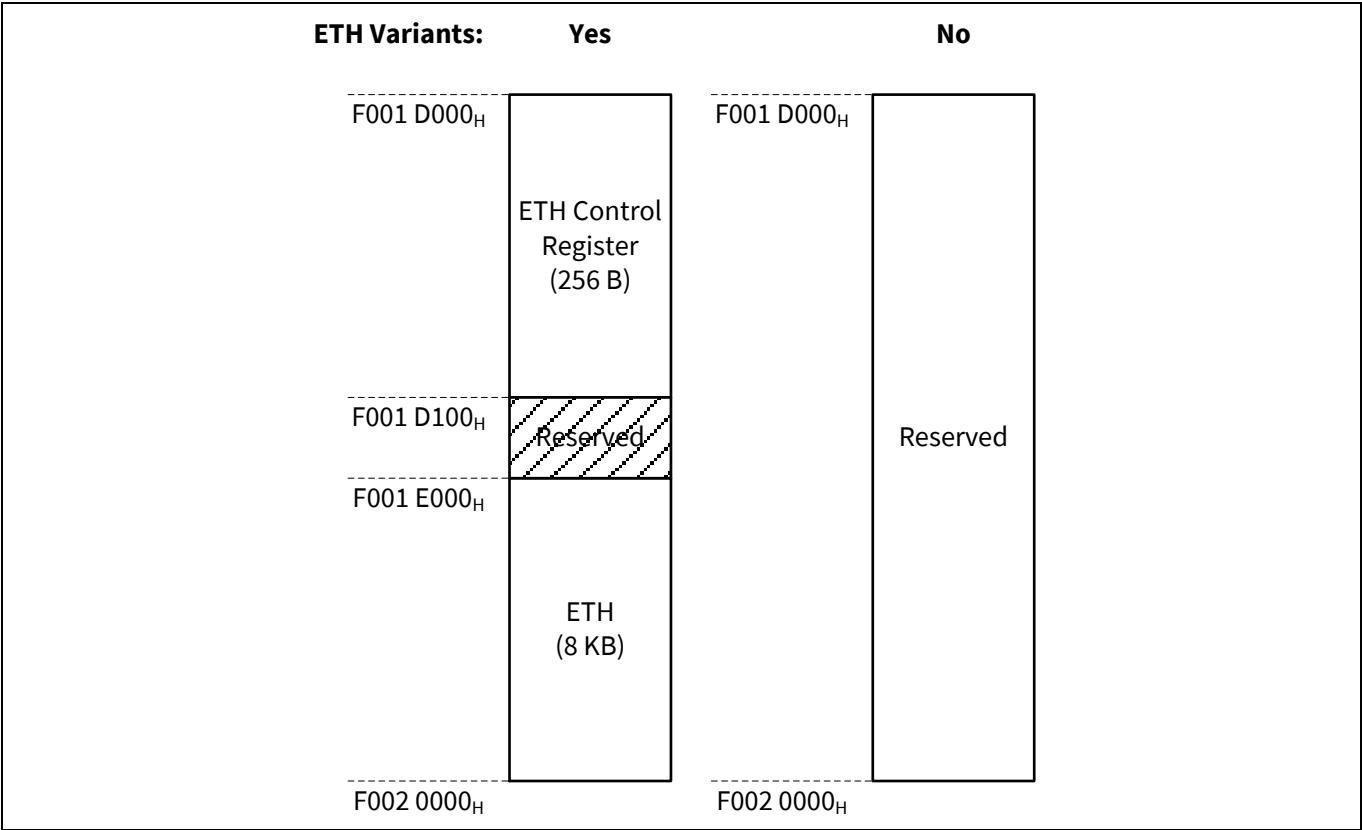


Figure 14 TC26x ETH variants

Memory map of variants

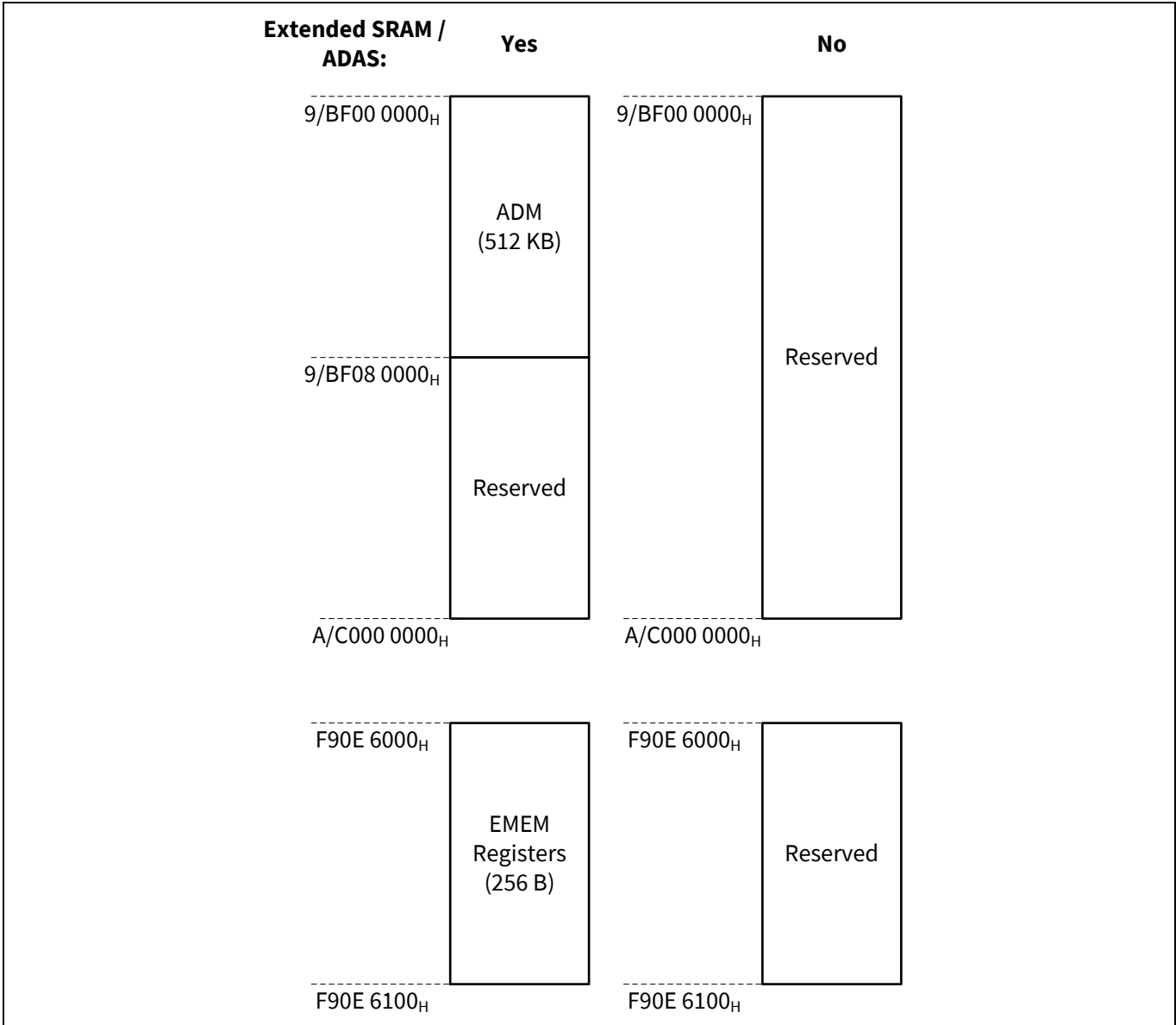


Figure 15 TC26x Extended SRAM / ADAS

Memory map of variants

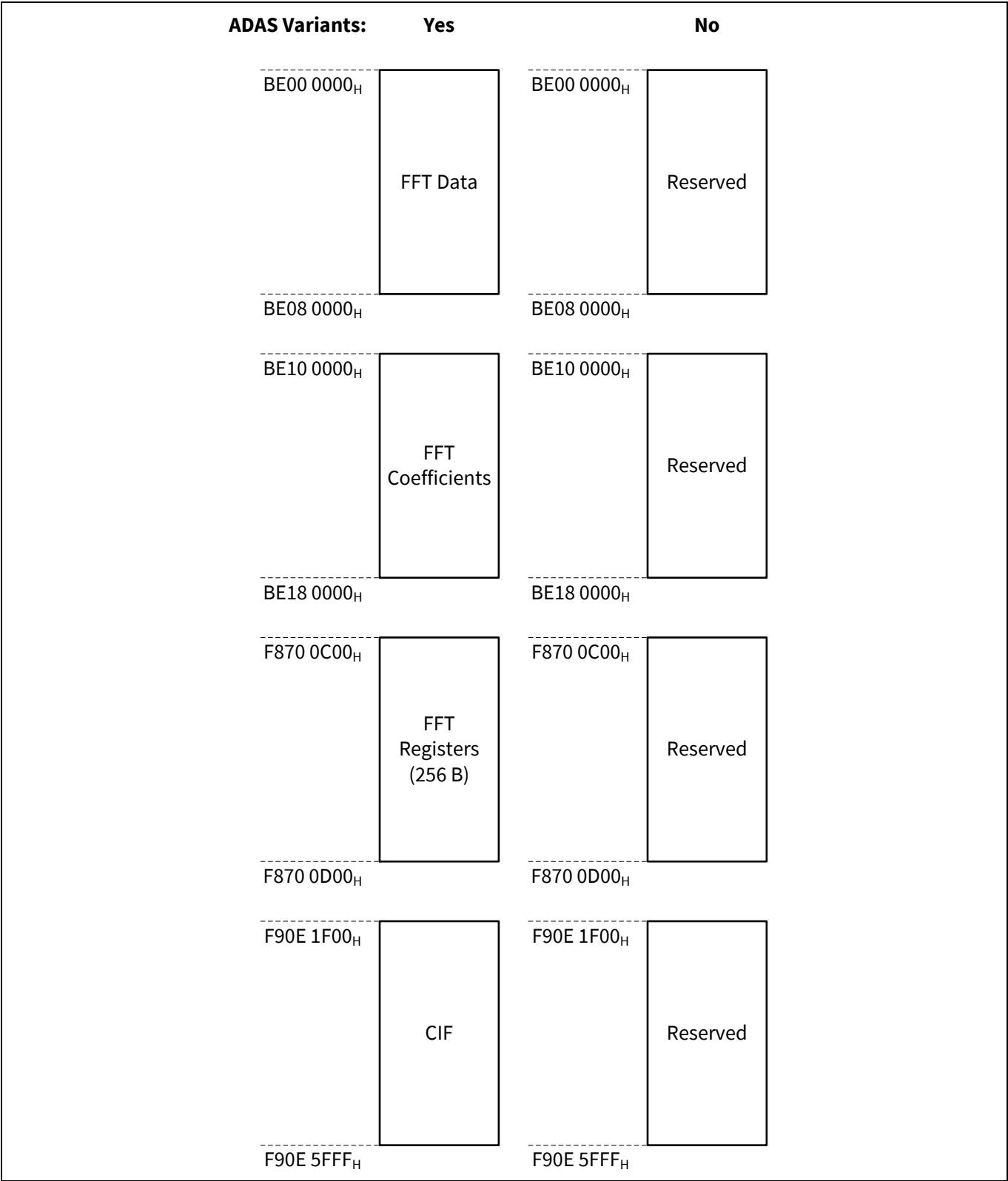


Figure 16 TC26x ADAS variants

CAN FD variants

No influence on Memory Map.

CAN FD = “No” variants: all CAN register fields NCRx.FDEN have to be kept at 0_B.

Memory map of variants

7.5 TC27x

DF_EEPROM Variants: 384 KB				144 KB			
Exemplary EEPROM size: 64 KB @ 500k				24 KB @ 500k			
AF00 0000 _H	Logical Sector	Size	Offset Address	AF00 0000 _H	Logical Sector	Size	Offset Address
	EEPROM0	8 KB	00 0000 _H		EEPROM0	8 KB	00 0000 _H
	EEPROM1	8 KB	00 2000 _H		EEPROM1	8 KB	00 2000 _H
	EEPROM2	8 KB	00 4000 _H		EEPROM2	8 KB	00 4000 _H
	...	...	...		...	...	...
AF06 0000 _H	EEPROM47	8 KB	05 E000 _H	AF06 0000 _H	EEPROM17	8 KB	02 2000 _H
					Reserved		

Figure 17 TC27x DF_EEPROM variants

Core1/2 PSPR Variants: 32 KB		24 KB	
5010 0000 _H	CPU2.PSPR (32 KB)	5010 0000 _H	CPU2.PSPR (24 KB)
		5010 6000 _H	Reserved
5010 8000 _H		5010 8000 _H	
6010 0000 _H	CPU1.PSPR (32 KB)	6010 0000 _H	CPU1.PSPR (24 KB)
		6010 6000 _H	Reserved
6010 8000 _H		6010 8000 _H	

Figure 18 TC27x Core1/2 PSPR variants

Memory map of variants

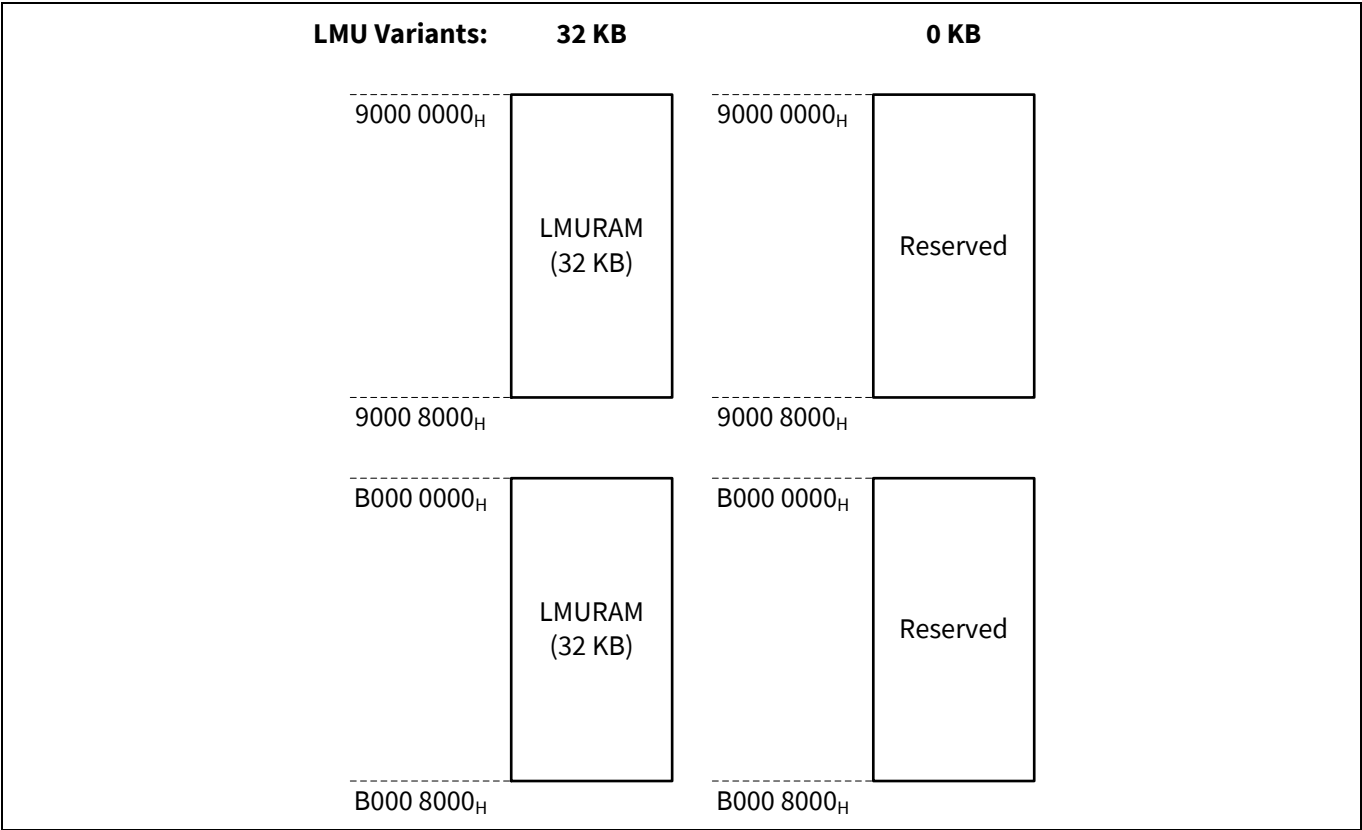


Figure 19 TC27x LMU variants

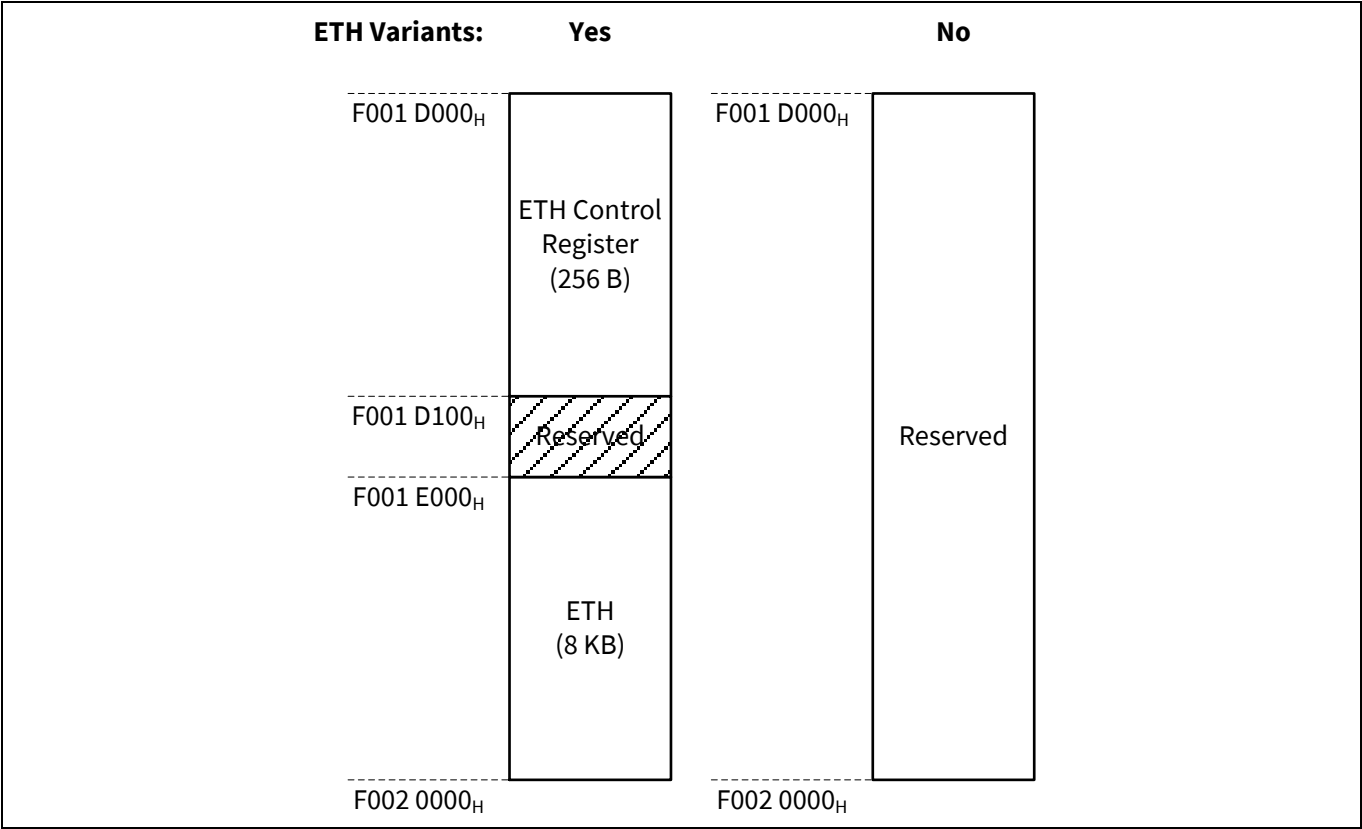


Figure 20 TC27x ETH variants

Memory map of variants

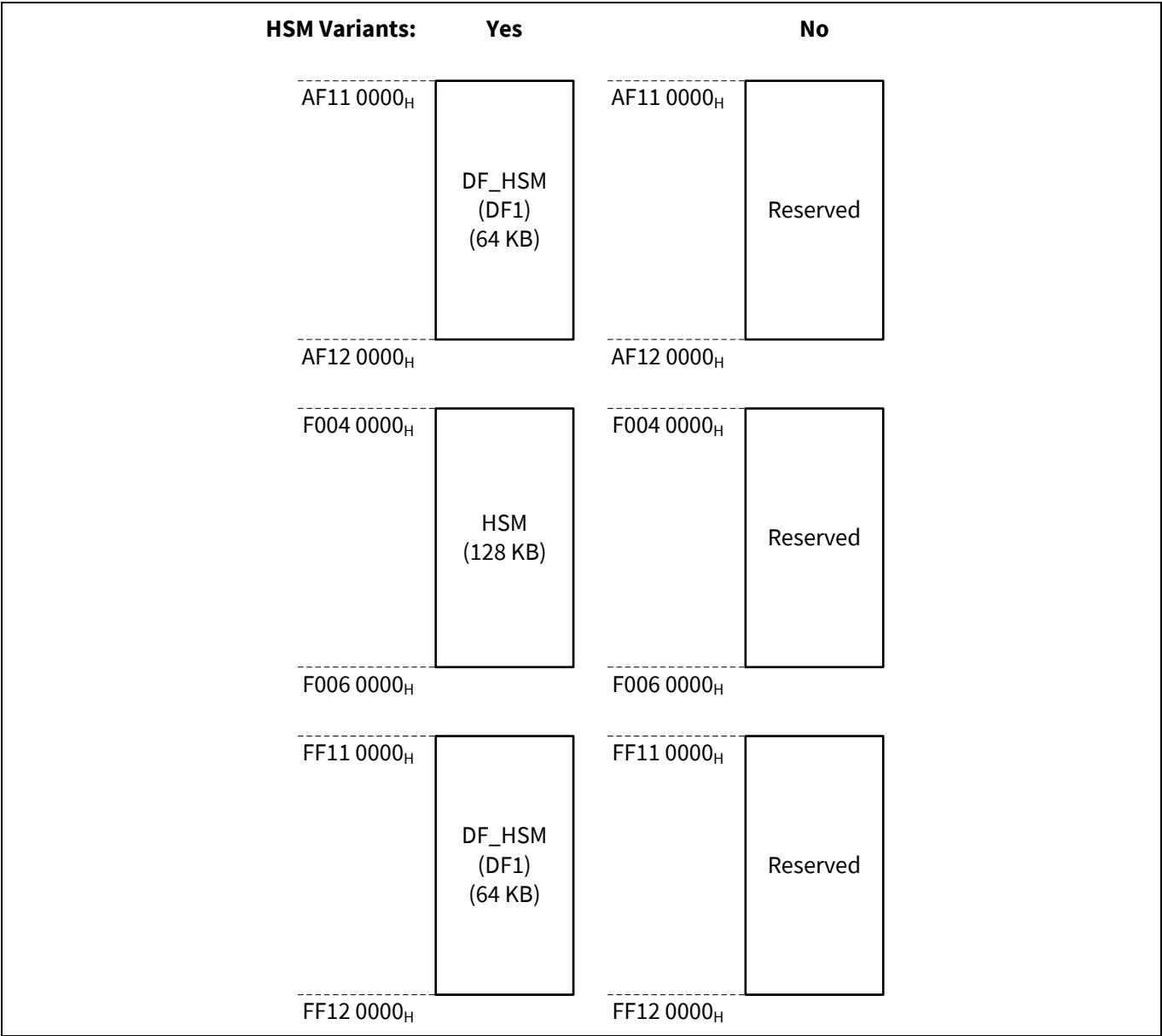


Figure 21 TC27x HSM variants

CAN FD variants

No influence on Memory Map.

CAN FD = “No” variants: all CAN register fields NCRx.FDEN have to be kept at 0_B

Memory map of variants

7.6 TC29x

				Sectorization of each 2 MB Bank			
PFlash Variants:	8 MB	6 MB	4 MB	Logical Sector	Phys. Sub-Sector	Size	Offset Address
8/A000 0000 _H	PFlash0 (2 MB)	PFlash0 (2 MB)	PFlash0 (2 MB)	S0	PS0 (512 KB)	16 KB	00 0000 _H
				S1		16 KB	00 4000 _H
				S2		16 KB	00 8000 _H
				S3		16 KB	00 C000 _H
				S4		16 KB	01 0000 _H
				S5		16 KB	01 4000 _H
				S6		16 KB	01 8000 _H
				S7		16 KB	01 C000 _H
8/A020 0000 _H	PFlash1 (2 MB)	PFlash1 (2 MB)	PFlash1 (2 MB)	S8		32 KB	02 0000 _H
				S9		32 KB	02 8000 _H
				S10		32 KB	03 0000 _H
				S11		32 KB	03 8000 _H
				S12		32 KB	04 0000 _H
				S13		32 KB	04 8000 _H
				S14		32 KB	05 0000 _H
				S15		32 KB	05 8000 _H
8/A040 0000 _H	PFlash2 (2 MB)	PFlash2 (2 MB)	Reserved	S16		64 KB	06 0000 _H
				S17		64 KB	07 0000 _H
				S18	PS1 (512 KB)	64 KB	08 0000 _H
				S19		64 KB	09 0000 _H
				S20		128 KB	0A 0000 _H
				S21		128 KB	0C 0000 _H
8/A060 0000 _H	PFlash3 (2 MB)	Reserved	Reserved	S22	PS2 (512 KB)	128 KB	0E 0000 _H
				S23		256 KB	10 0000 _H
				S24	PS3 (512 KB)	256 KB	14 0000 _H
				S25		256 KB	18 0000 _H
8/A080 0000 _H				S26		256 KB	1C 0000 _H

Figure 22 TC29x PFlash variants

Memory map of variants

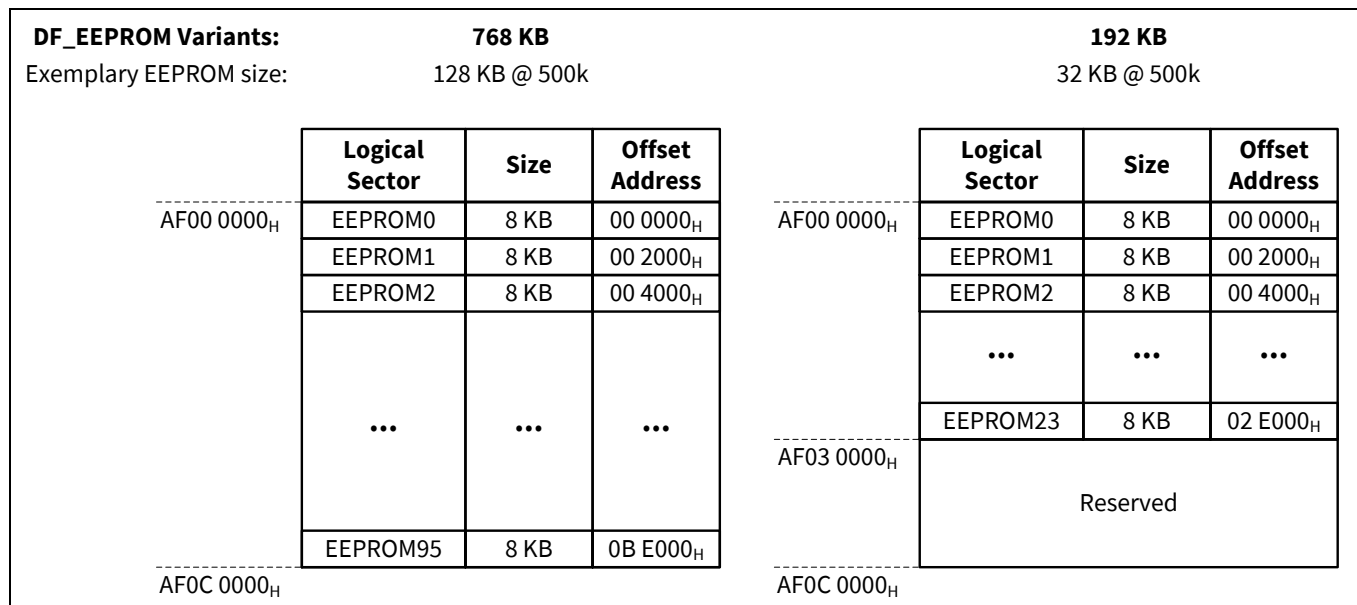


Figure 23 TC29x DF_EEPROM variants

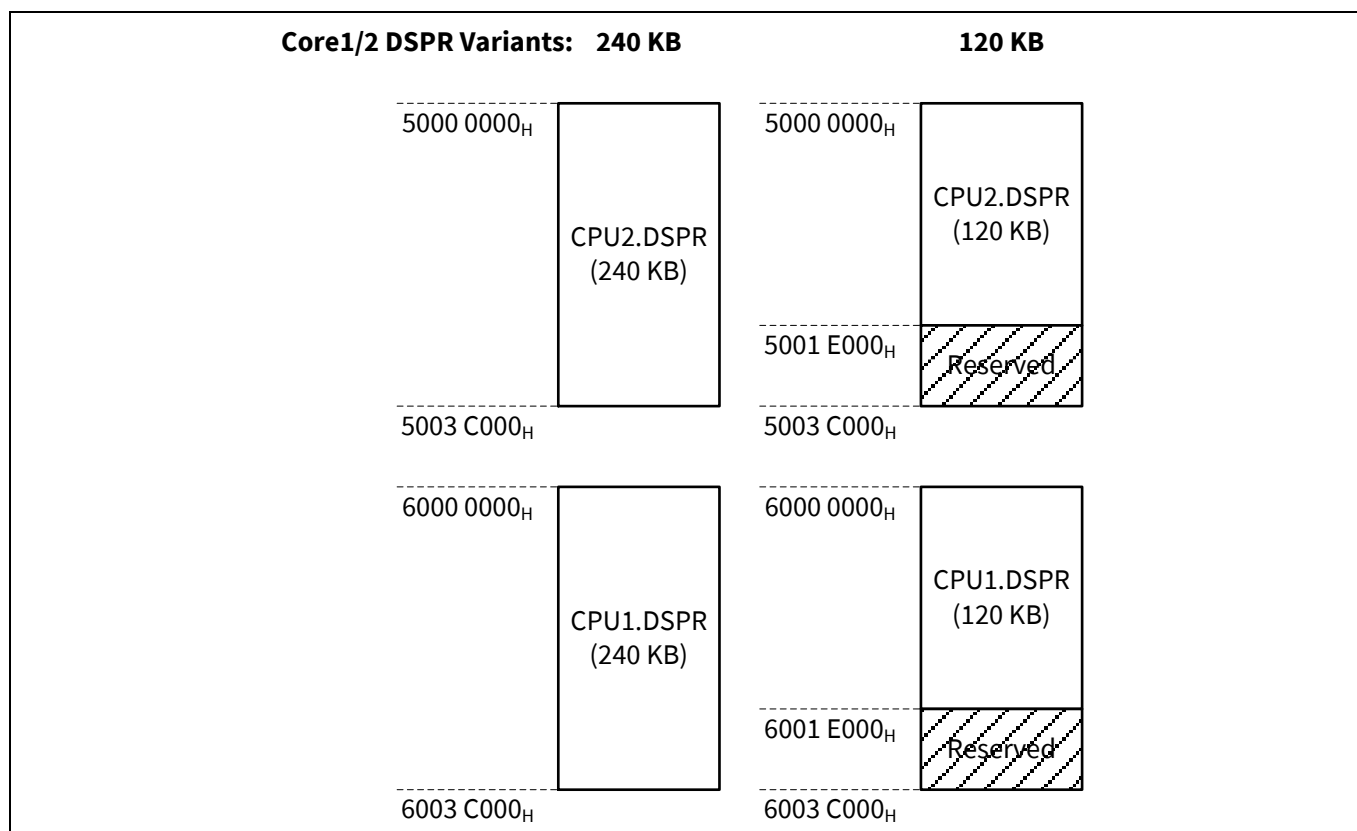


Figure 24 TC29x Core1/2 DSPR variants

Memory map of variants

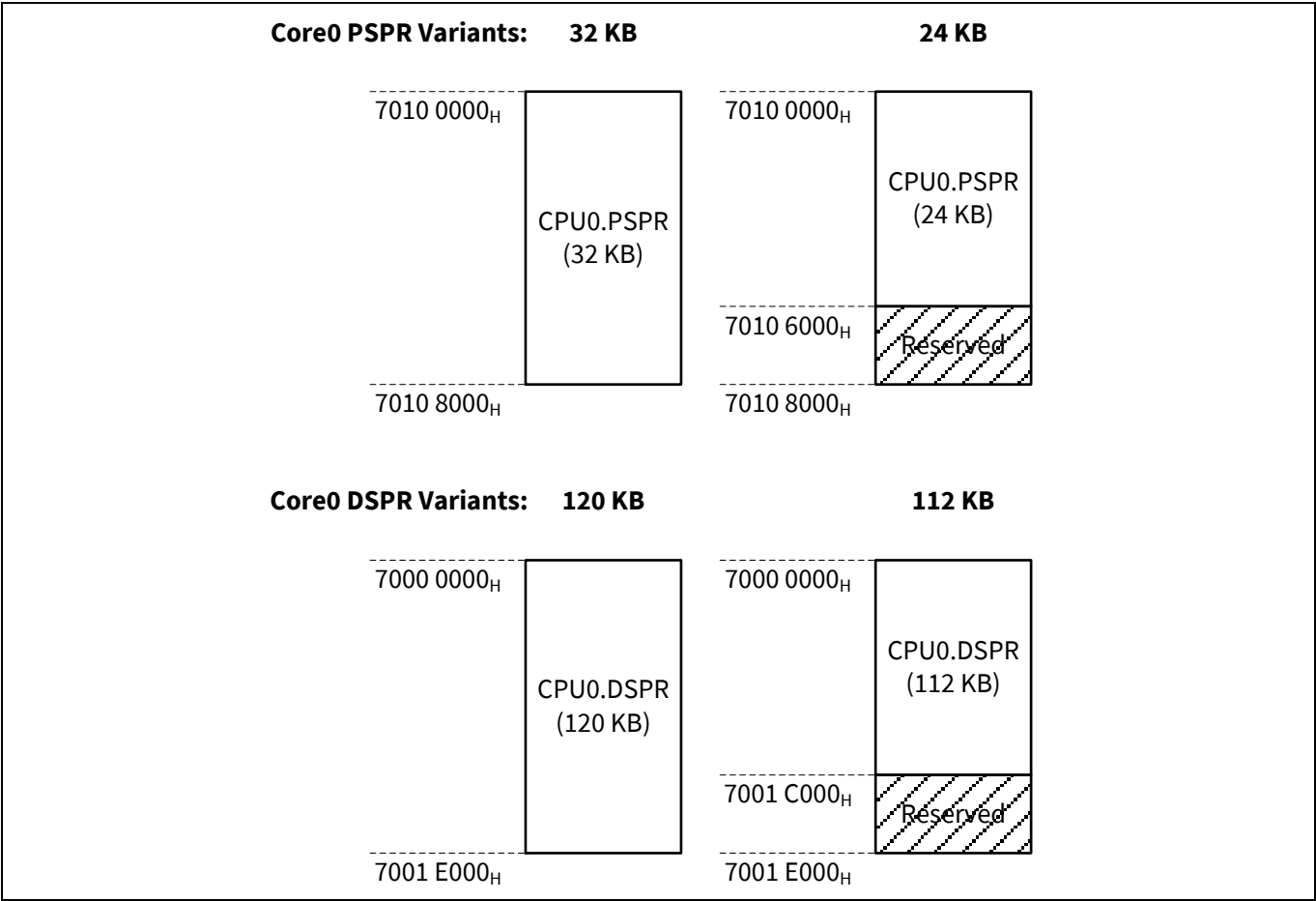


Figure 25 TC29x Core0 PSPR / DSPR variants

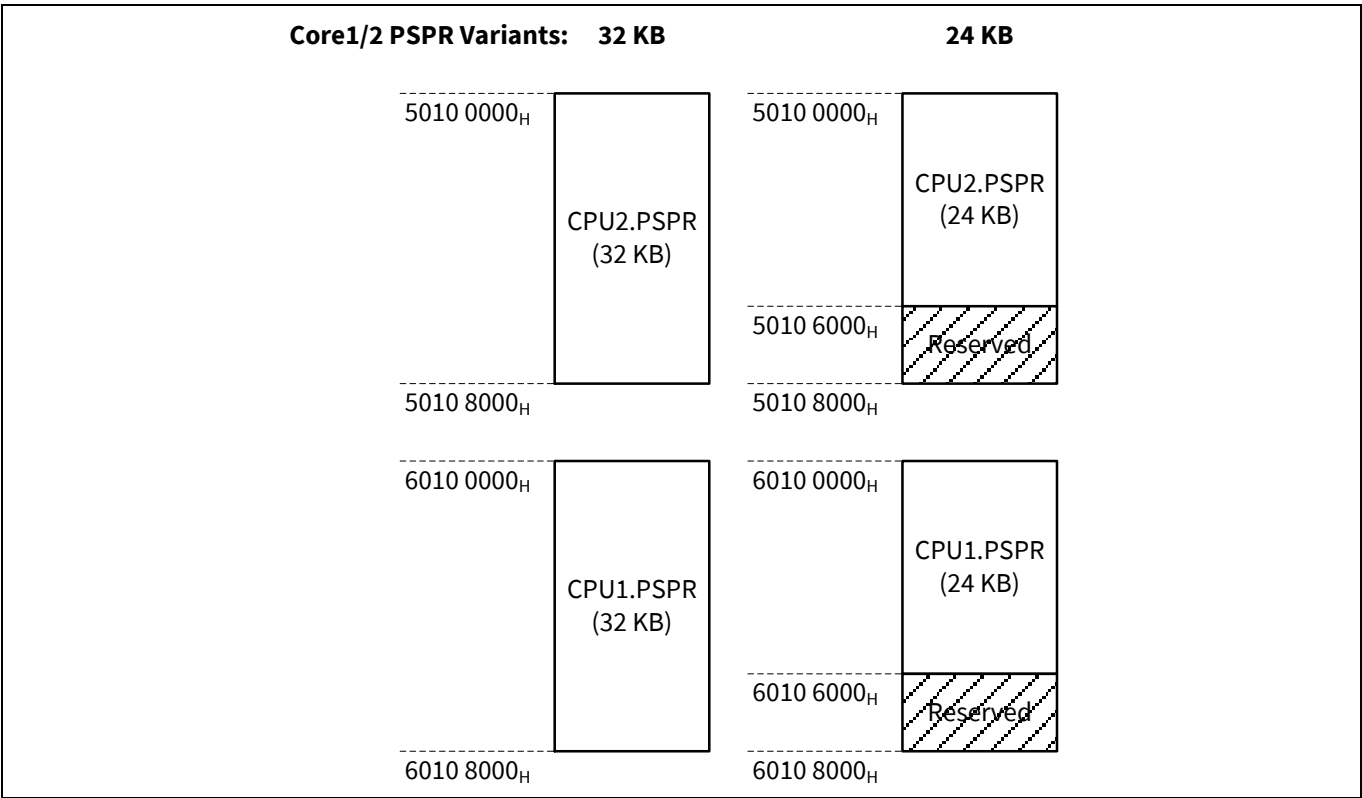


Figure 26 TC29x Core1/2 PSPR variants

Memory map of variants

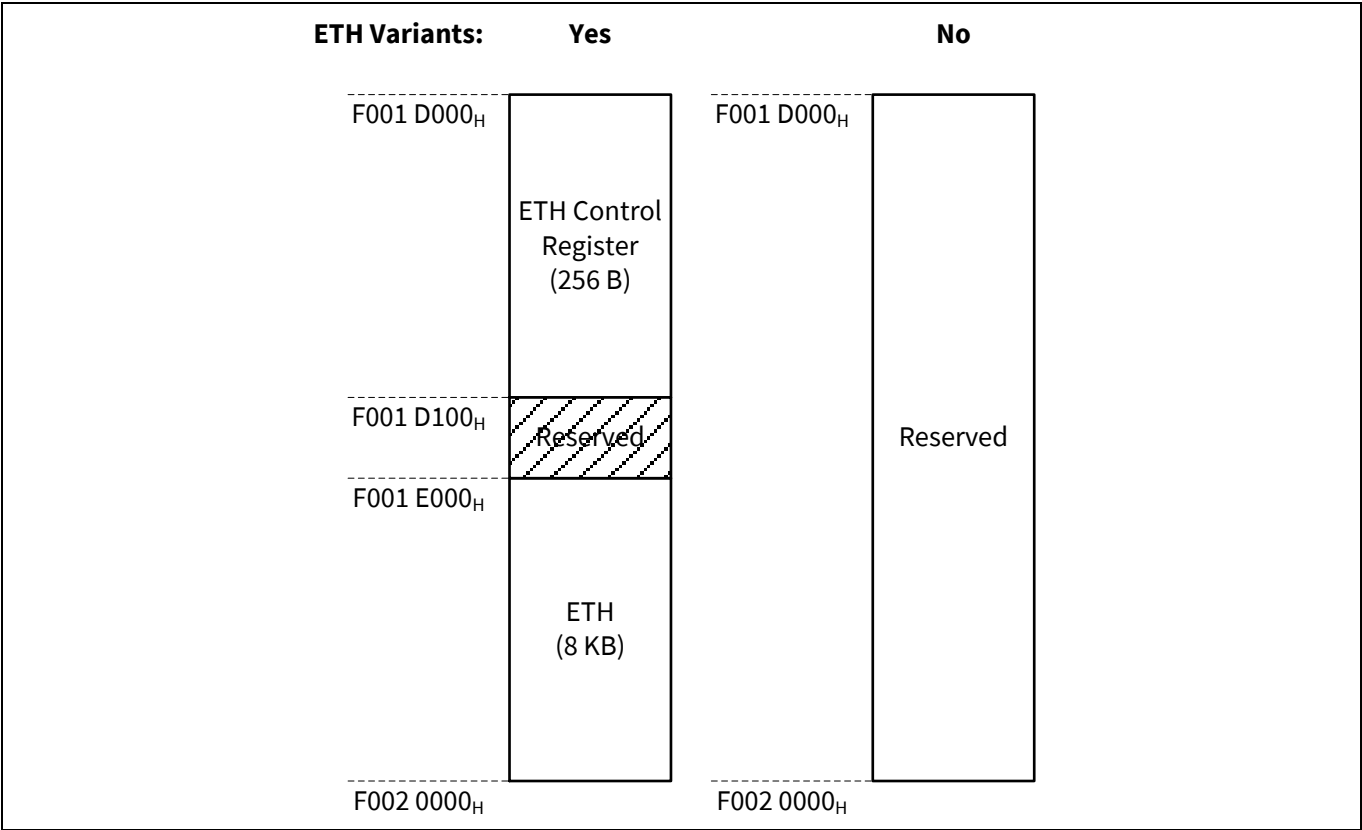


Figure 27 TC29x ETH variants

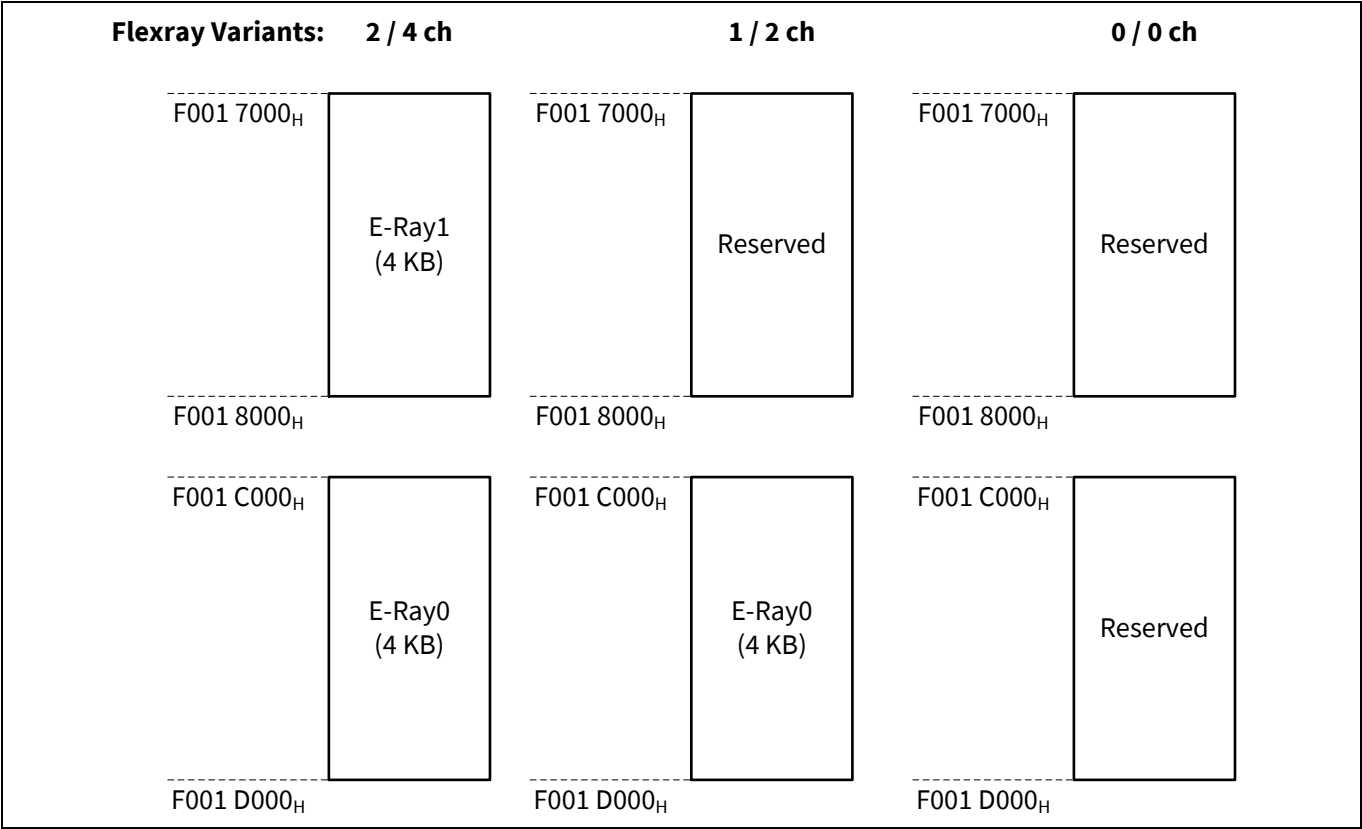


Figure 28 TC29x FlexRay variants

Memory map of variants

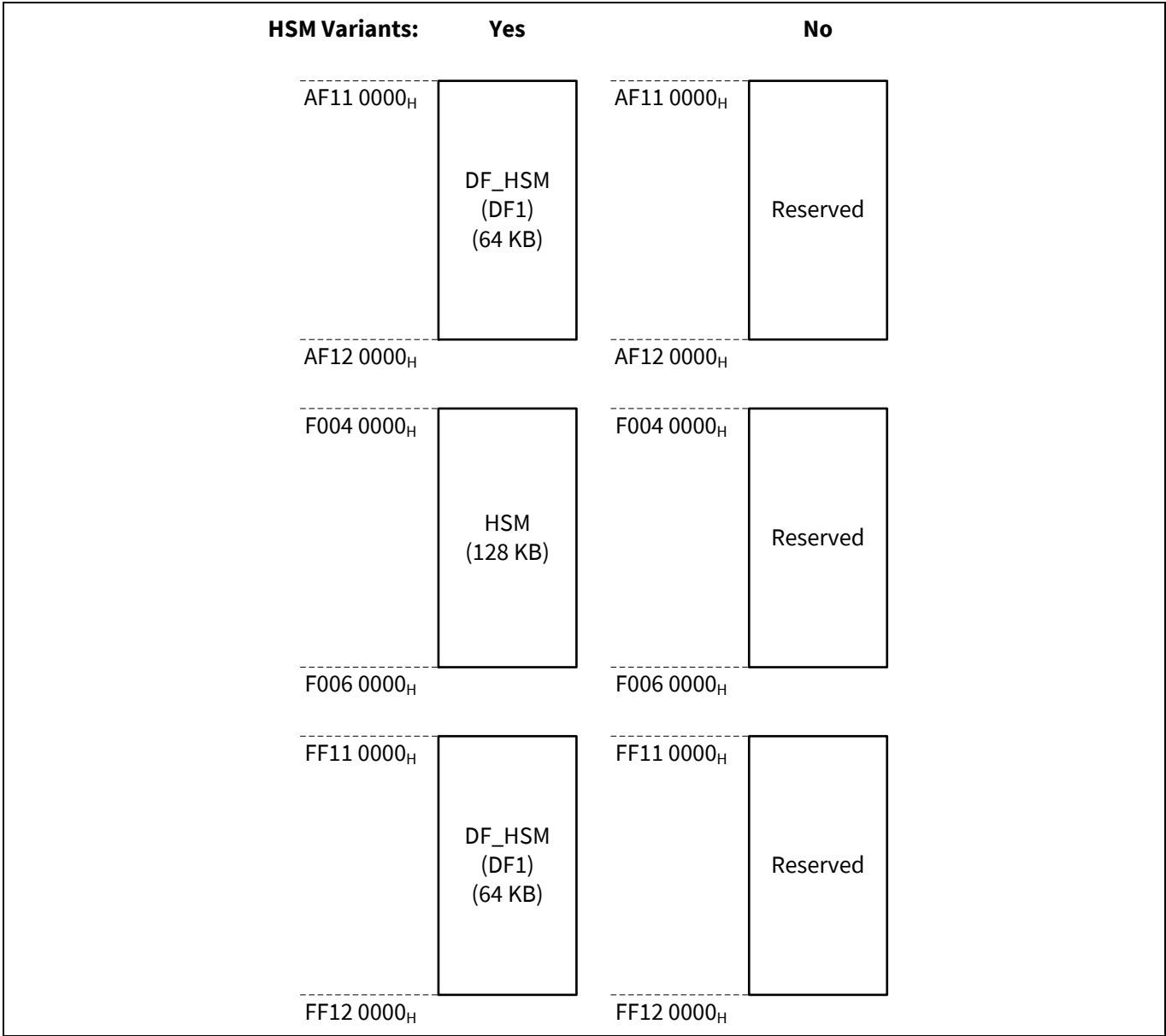


Figure 29 TC29x HSM variants

Memory map of variants

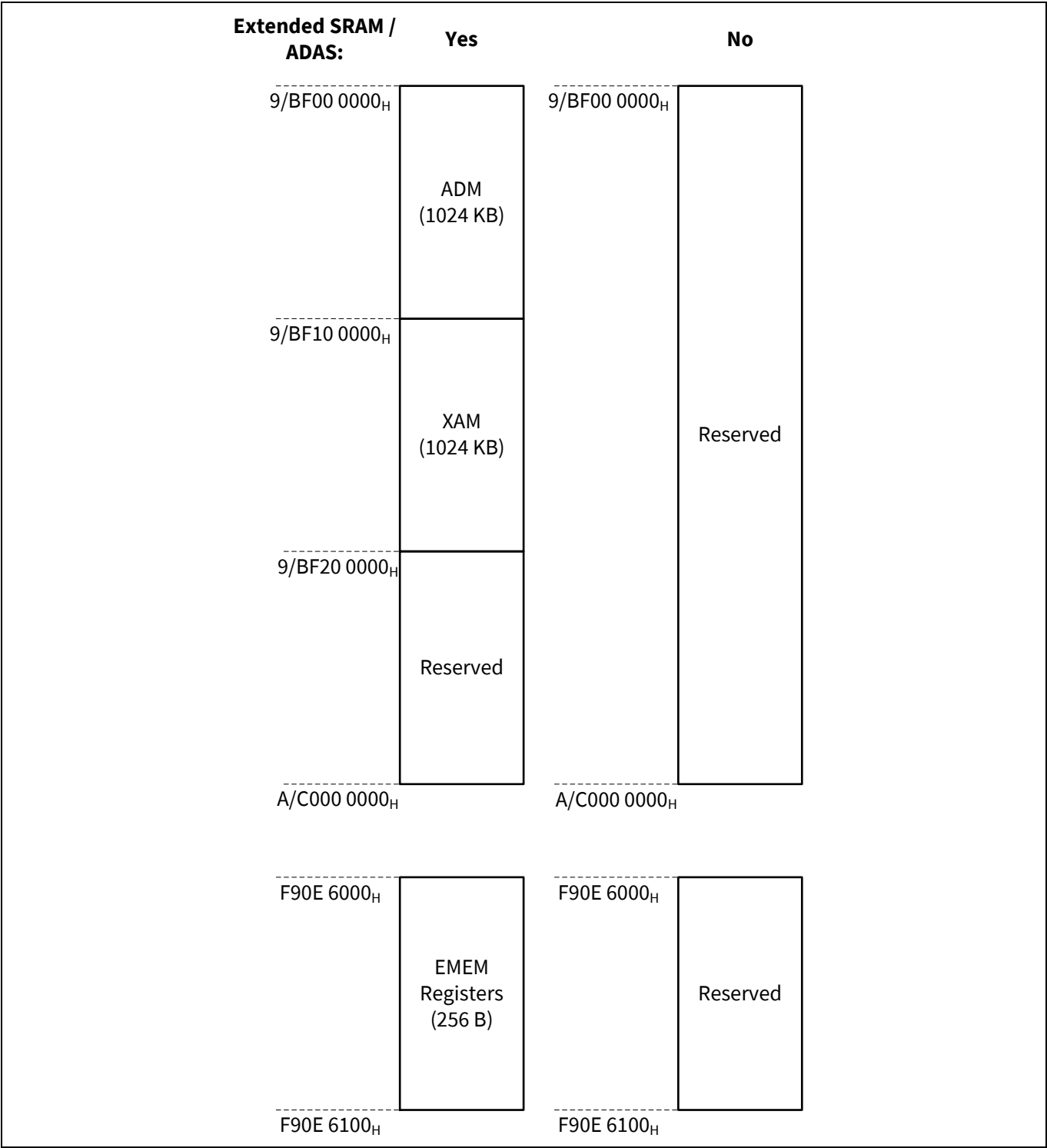


Figure 30 TC29x extended SRAM / ADAS

Memory map of variants

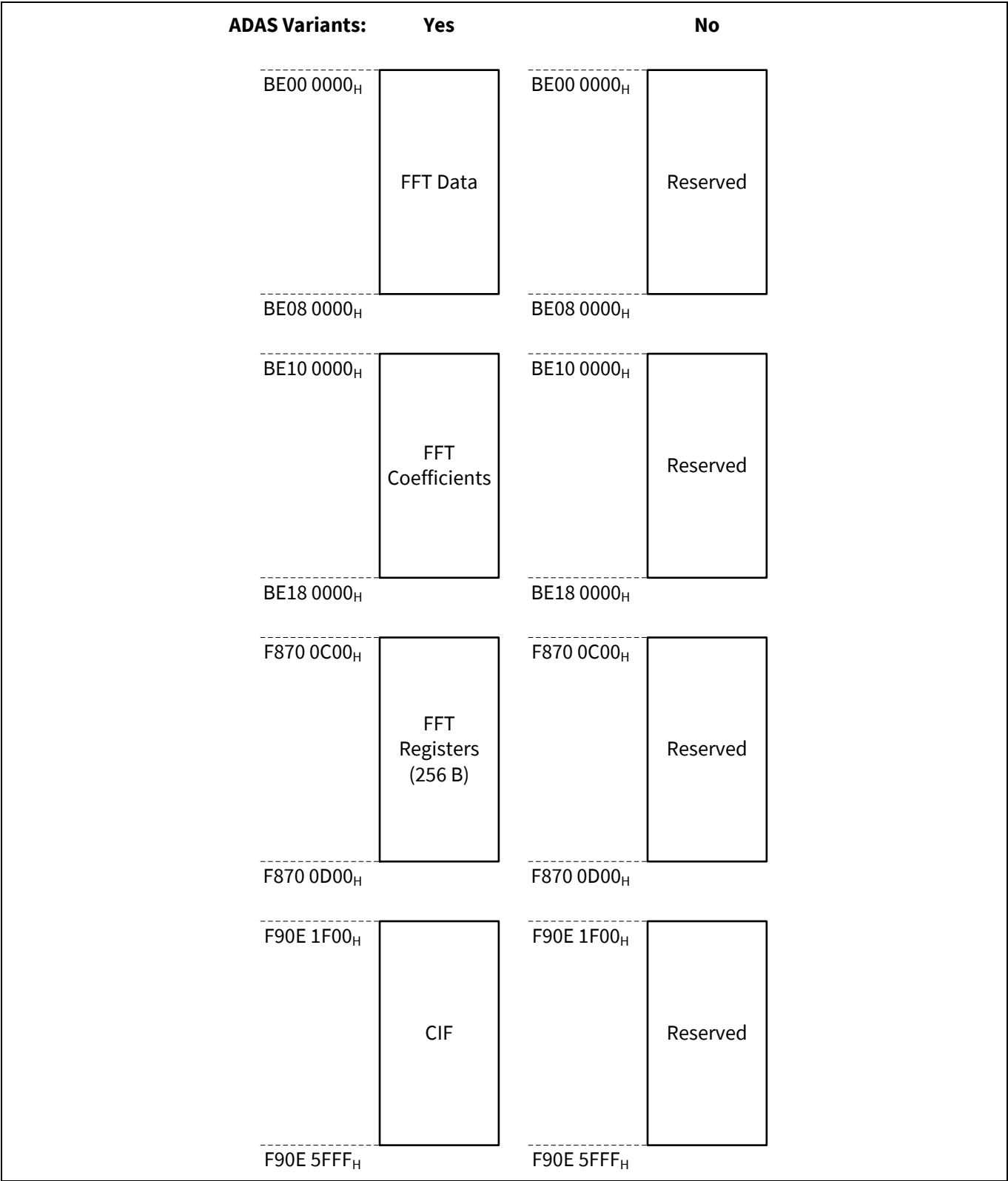


Figure 31 TC29x ADAS variants

CAN FD Variants

No influence on Memory Map.

CAN FD = “No” variants: all CAN register fields NCRx.FDEN have to be kept at 0_B

Revision history

Revision history

Major changes since the last revision

Page or reference	Description of change
V1.0	First release

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2019-03

Published by

Infineon Technologies AG

81726 Neubiberg, Germany

© 2019 Infineon Technologies AG.

All Rights Reserved.

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

ifxDSA0002

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the type in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof could reasonably be expected to result in personal injury.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Infineon:

[TC237L32F200SACKXUMA1](#) [TC234LP32F200FACKXUMA1](#) [TC234L32F200FACKXUMA1](#)
[TC233LP32F200NACKXUMA1](#) [TC237LP32F200SACKXUMA1](#) [TC233LP32F200FACKXUMA1](#)
[TC237LP32F200NACKXUMA1](#) [TC233L32F200NACKXUMA1](#) [TC234LP32F200NACKXUMA1](#)
[TC234L32F200NACKXUMA1](#) [TC299TP128F300NBCLXUMA1](#) [TC297TA128F300NBCKXUMA1](#)
[TC299T128F300SBCKXUMA1](#) [TC299TX128F300SBCKXUMA1](#) [TC299TP128F300SBCKXUMA1](#)
[TC297TA128F300SBCKXUMA1](#) [TC297TX128F300SBCKXUMA1](#) [TC297TX128F300NBCKXUMA1](#)
[TC299TX128F300NBCKXUMA1](#) [TC297TP128F300NBCKXUMA1](#) [TC297TA64F300SBCKXUMA1](#)
[TC297TP128F300SBCKXUMA1](#) [TC299TP128F300NBCKXUMA1](#) [TC233LP32F200NACLXUMA1](#)
[TC213L8F133NACKXUMA1](#) [TC213L8F133NACLXUMA1](#) [TC237LP32F200NACLXUMA1](#)
[TC267D40F200NBCLXUMA1](#) [TC267D40F200NBCKXUMA1](#) [TC297TX128F300SBCKXUMA2](#)
[TC299TP128F300SBCKXUMA2](#) [TC297TX128F300NBCKXUMA2](#) [TC299TP128F300NBCLXUMA2](#)
[TC265D40F200NBCKXUMA1](#) [TC264D40F200NBCKXUMA2](#) [TC264D40F200NBCLXUMA1](#)
[TC212S8F133NACKXUMA1](#) [TC214L8F133NACKXUMA1](#) [TC222L16F133NACKXUMA1](#) [TC222L16F133NACLXUMA1](#)
[TC222S16F133NACKXUMA1](#) [TC223L16F133NACKXUMA1](#) [TC224L16F133NACKXUMA1](#)
[TC212L8F133NACKXUMA1](#) [TC212L8F133NACLXUMA1](#) [TC264DA40F200WBCKXUMA1](#)
[TC233L32F200FACKXUMA1](#) [TC233LP32F200FACLXUMA1](#) [TC237LP32F200SACLXUMA1](#)
[TC212L8F133FACKXUMA1](#) [TC213L8F133FACKXUMA1](#) [TC223L16F133FACKXUMA1](#) [TC223L16F133NACLXUMA1](#)
[TC223S16F133FACKXUMA1](#) [TC223S16F133FACLXUMA1](#) [TC224L16F133NACLXUMA1](#)
[TC237L32F200SACLXUMA1](#) [TC298TP128F300NBCLXUMA2](#) [TC212S8F133FACKXUMA1](#)
[TC222L16F133FACKXUMA1](#) [TC222S16F133FACKXUMA1](#) [TC224L16F133FACLXUMA1](#)
[TC233L32F200FACLXUMA1](#) [TC264D40F200WBCKXUMA1](#) [TC265D40F200NBCLXUMA1](#)
[TC265D40F200WBCKXUMA1](#) [TC267D40F200SBCKXUMA1](#) [TC264DA40F200NBCKXUMA2](#)
[TC212S8F133SCACKXUMA1](#) [TC297TA128F300SBCKXUMA2](#) [TC299TP128F300NBCKXUMA2](#)