

OptiMOS™-5 Power-Transistor



Features

- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal Level
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Quality Features

- Infineon Automotive Quality
- Extended qualification beyond AEC Q101
- Enhanced testing
- Advanced adhesion against delamination
- Complementary testing for board level reliability



Advanced
adhesion



Robust

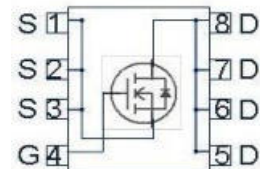
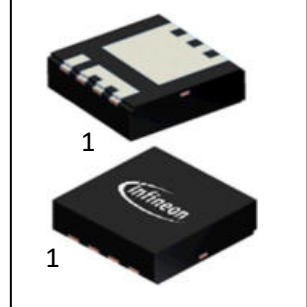


Enhanced
tested

Product Summary

V_{DS}	80	V
$R_{DS(on)}$	10	mΩ
I_D	40	A

PG-TSDSON-8



Type	Package	Marking
IAUZ40N08S5N100	PG-TSDSON-8	5N08100

Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}, V_{GS}=10\text{ V}^{(1)}$	40	A
		$T_C=100\text{ °C}, V_{GS}=10\text{ V}^{(2)}$	40	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	160	
Avalanche energy, single pulse ⁽²⁾	E_{AS}	$I_D=20\text{ A}$	75	mJ
Avalanche current, single pulse	I_{AS}	-	32	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	68	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	2.2	K/W
Thermal resistance, junction - ambient ³⁾	R_{thJA}		-	38.5	-	

Electrical characteristics, at $T_j=25\text{ }^{\circ}\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=27\text{ }\mu\text{A}$	2.2	3	3.8	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^{\circ}\text{C}$	-	-	1	μA
		$V_{DS}=80\text{ V}, V_{GS}=0\text{ V}, T_j=85\text{ }^{\circ}\text{C}^{2)}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=6\text{ V}, I_D=10\text{ A}$	-	11.6	14.5	m Ω
		$V_{GS}=10\text{ V}, I_D=20\text{ A}$	-	8.4	10	
Gate resistance ²⁾	R_G		-	1.2	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=40\text{ V},$ $f=1\text{ MHz}$	-	1224	1591	pF
Output capacitance	C_{oss}		-	231	300	
Reverse transfer capacitance	C_{rss}		-	13.5	20	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=40\text{ A}, R_G=3.5\ \Omega$	-	3	-	ns
Rise time	t_r		-	1	-	
Turn-off delay time	$t_{d(off)}$		-	7	-	
Fall time	t_f		-	5	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=40\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	5.8	7.5	nC
Gate to drain charge	Q_{gd}		-	4.5	6.8	
Gate charge total	Q_g		-	18.6	24.2	
Gate plateau voltage	$V_{plateau}$		-	4.8	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25\text{ °C}$	-	-	40	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	147	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=20\text{ A},$ $T_J=25\text{ °C}$	-	0.9	1.2	V
Reverse recovery time ²⁾	t_{rr}	$V_R=40\text{ V}, I_F=40\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	37	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	32	-	nC

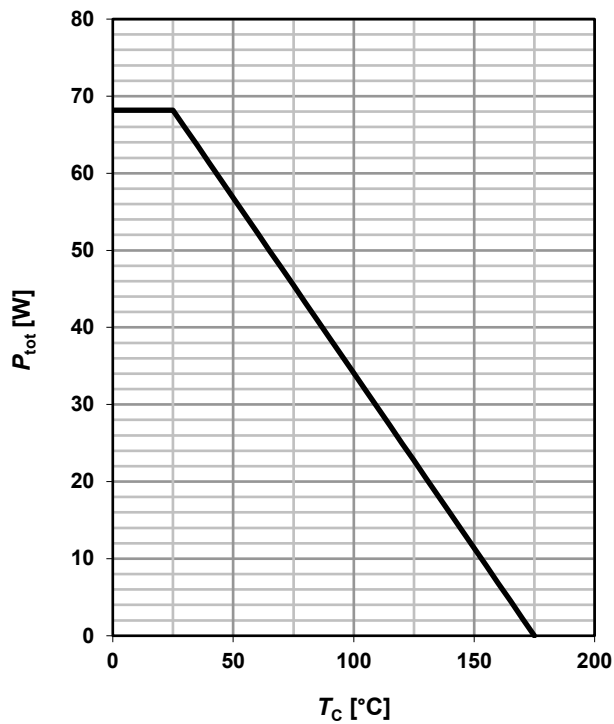
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 2.2\text{ K/W}$ the chip is able to carry 58A at 25°C.

²⁾ The parameter is not subject to production test - verified by design/characterization.

³⁾ Device on four layer 2s2p PCB defined in accordance with JEDEC standards (JESD51-5-7).
PCB is vertical in still air.

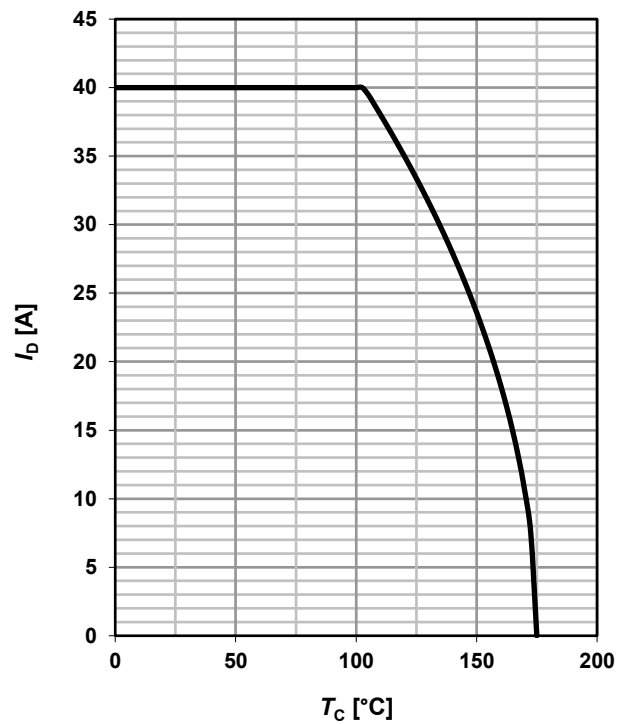
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

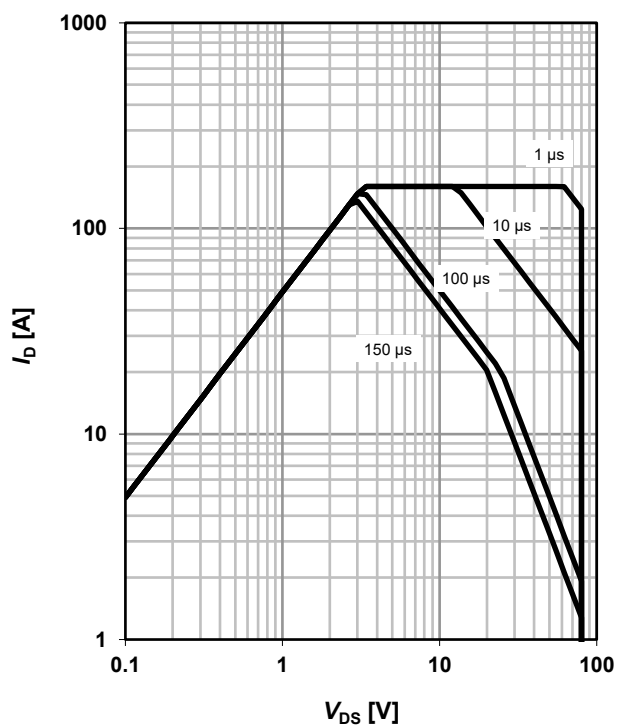
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

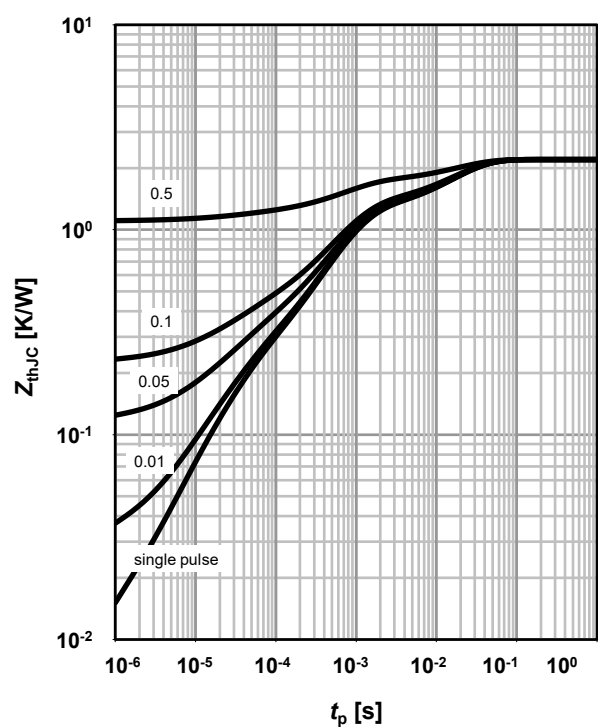
parameter: t_p



4 Max. transient thermal impedance

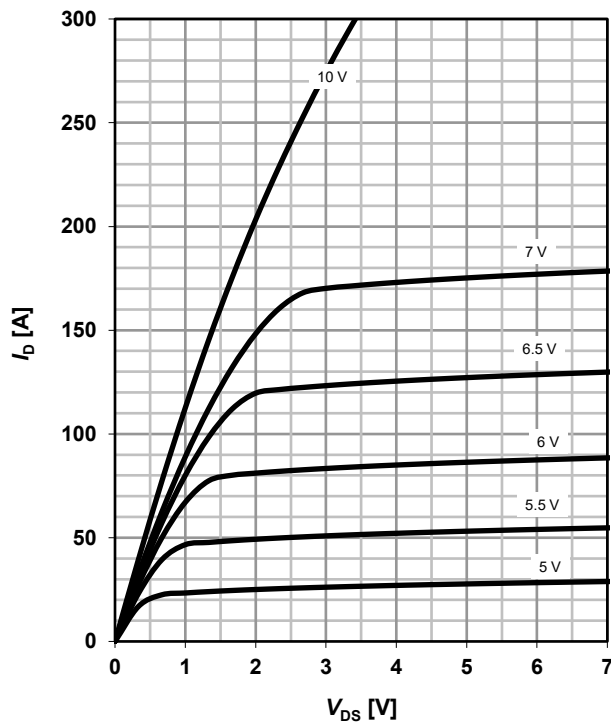
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



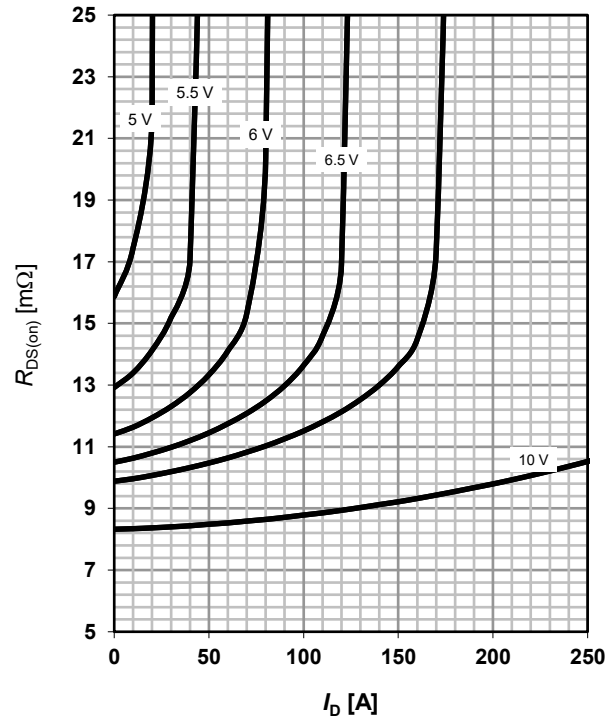
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


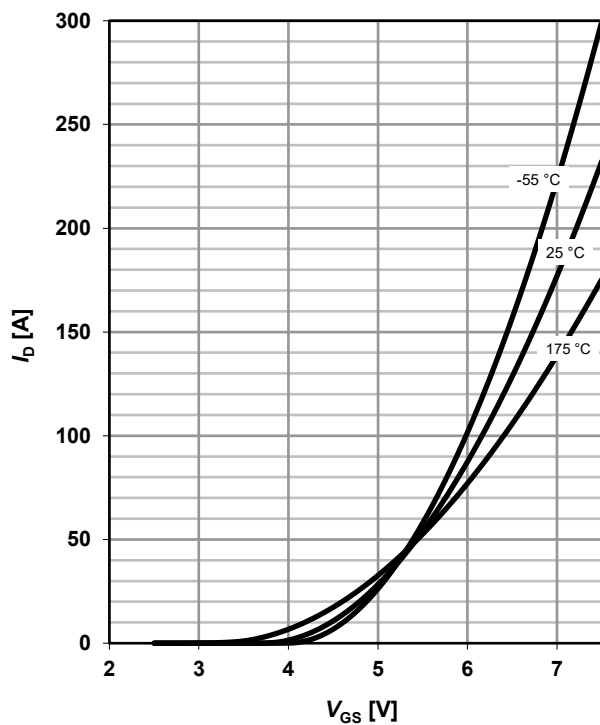
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

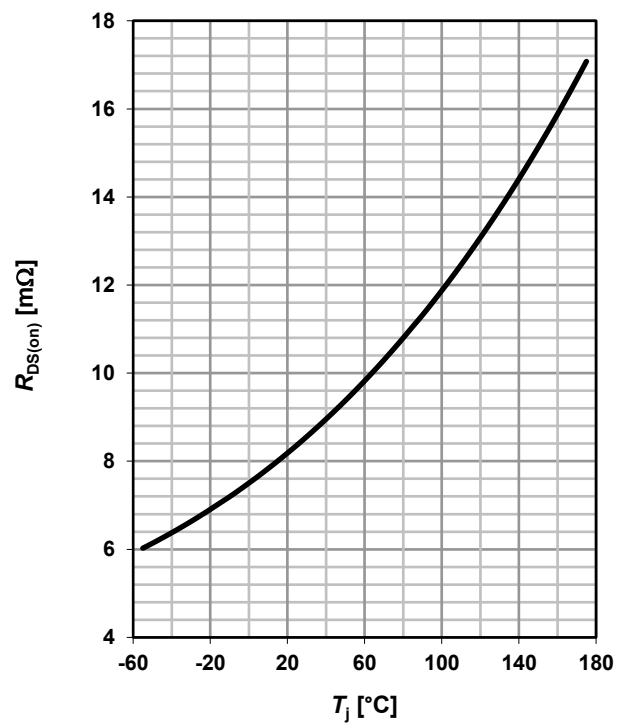
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter: T_j


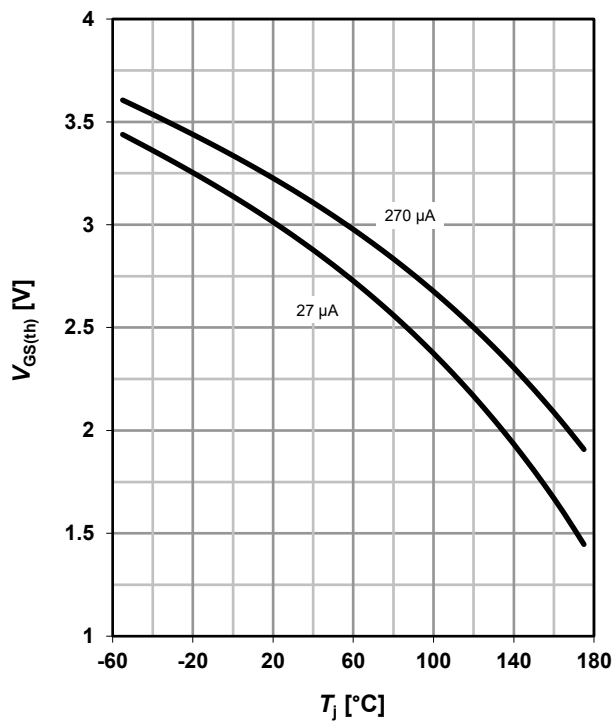
8 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(T_j); I_D = 20\text{ A}; V_{GS} = 10\text{ V}$


9 Typ. gate threshold voltage

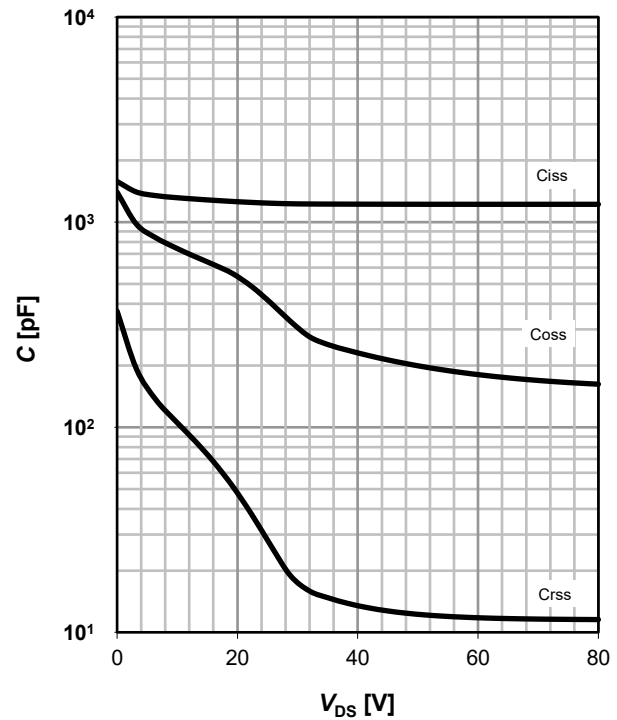
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

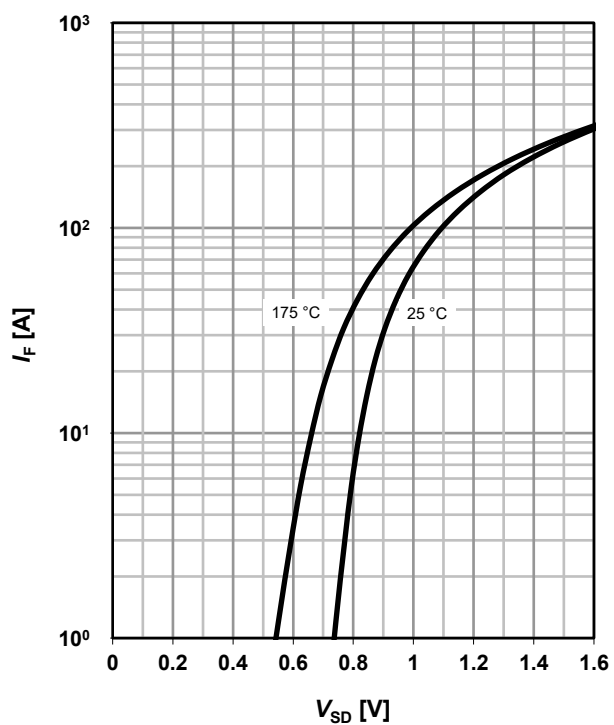
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

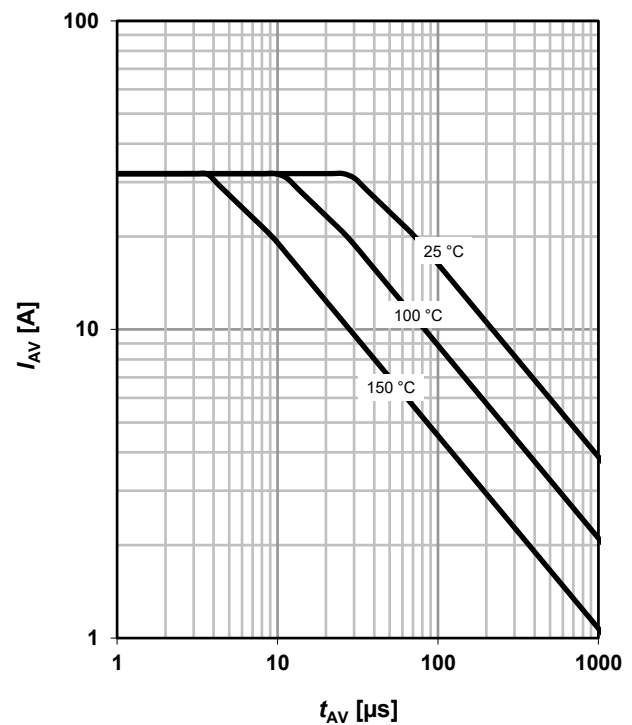
parameter: T_j



12 Typ. avalanche characteristics

$$I_{AS} = f(t_{AV})$$

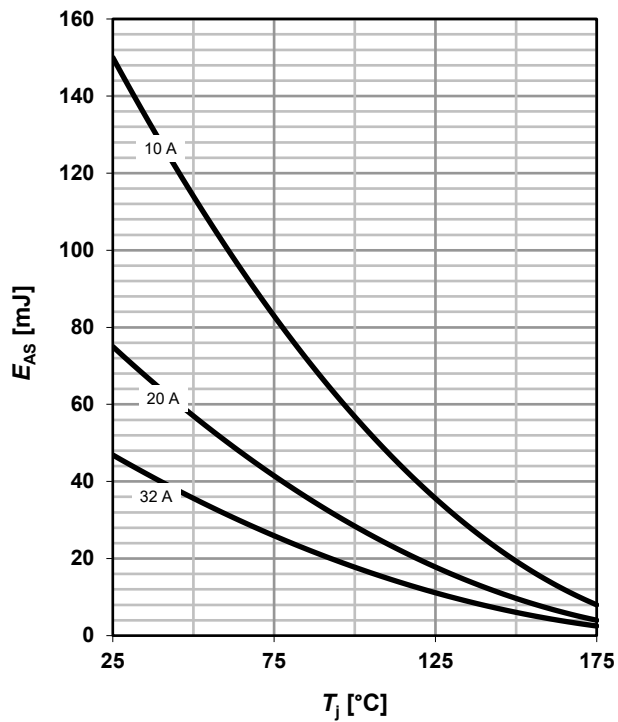
parameter: $T_{j(start)}$



13 Typical avalanche energy

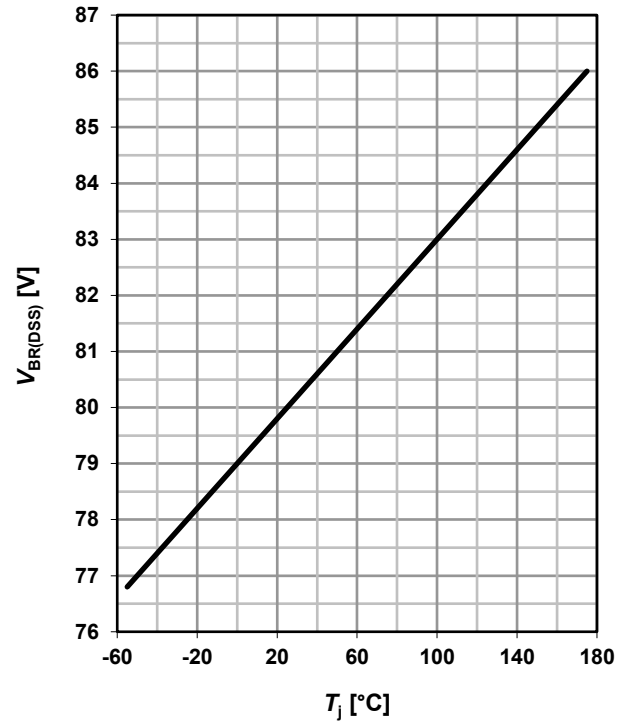
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

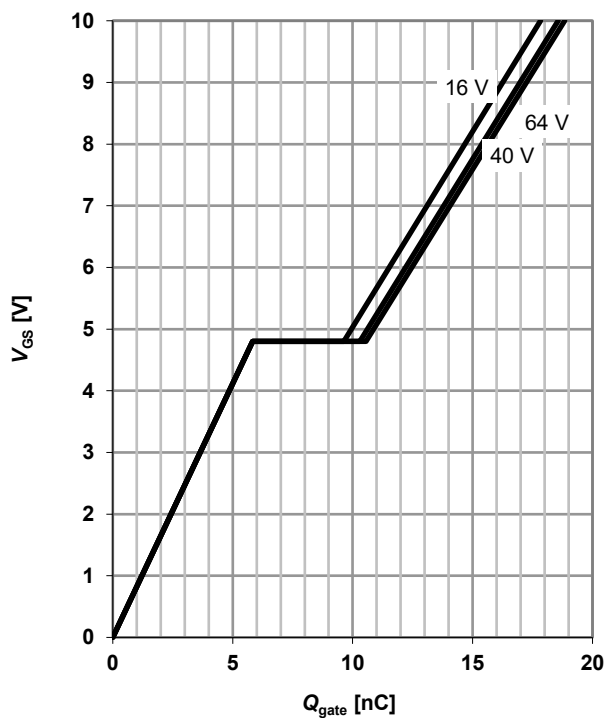
$$V_{BR(DSS)} = f(T_j); I_{D_typ} = 1 \text{ mA}$$



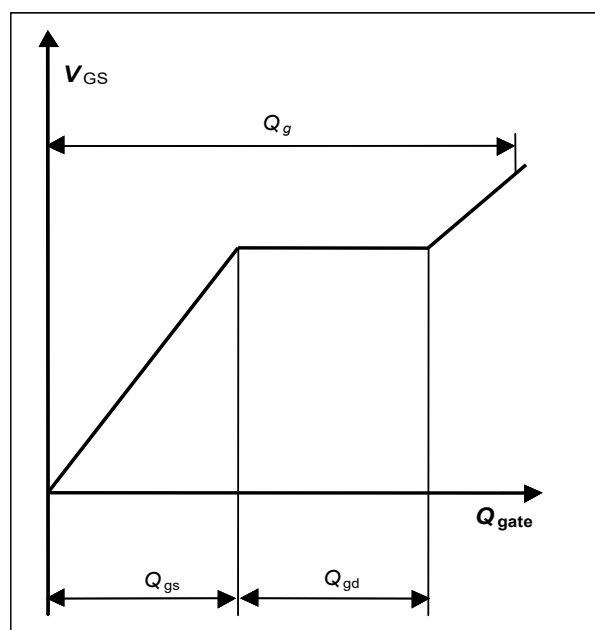
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 20 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



[illegible]

Figure 1 shows the dimensions of the stencil. The top view (left) and side view (right) are provided. The top view shows a rectangular stencil with a central rectangular opening and four smaller rectangular openings at the corners. The dimensions are as follows:

- Overall width: 2.29
- Overall height: 2.36
- Central opening width: 1.64
- Central opening height: 1.45
- Corner opening width: 0.34
- Corner opening height: 0.45

The side view shows the thickness of the stencil, which is 0.07. The side view also shows the dimensions of the central opening, which is 1.09 wide and 1.4 high. The side view also shows the dimensions of the four corner openings, which are 0.31 wide and 0.6 high.

Legend:

- Copper
- Solder Mask
- Stencil Apertures

[illegible]

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